FIG. 1

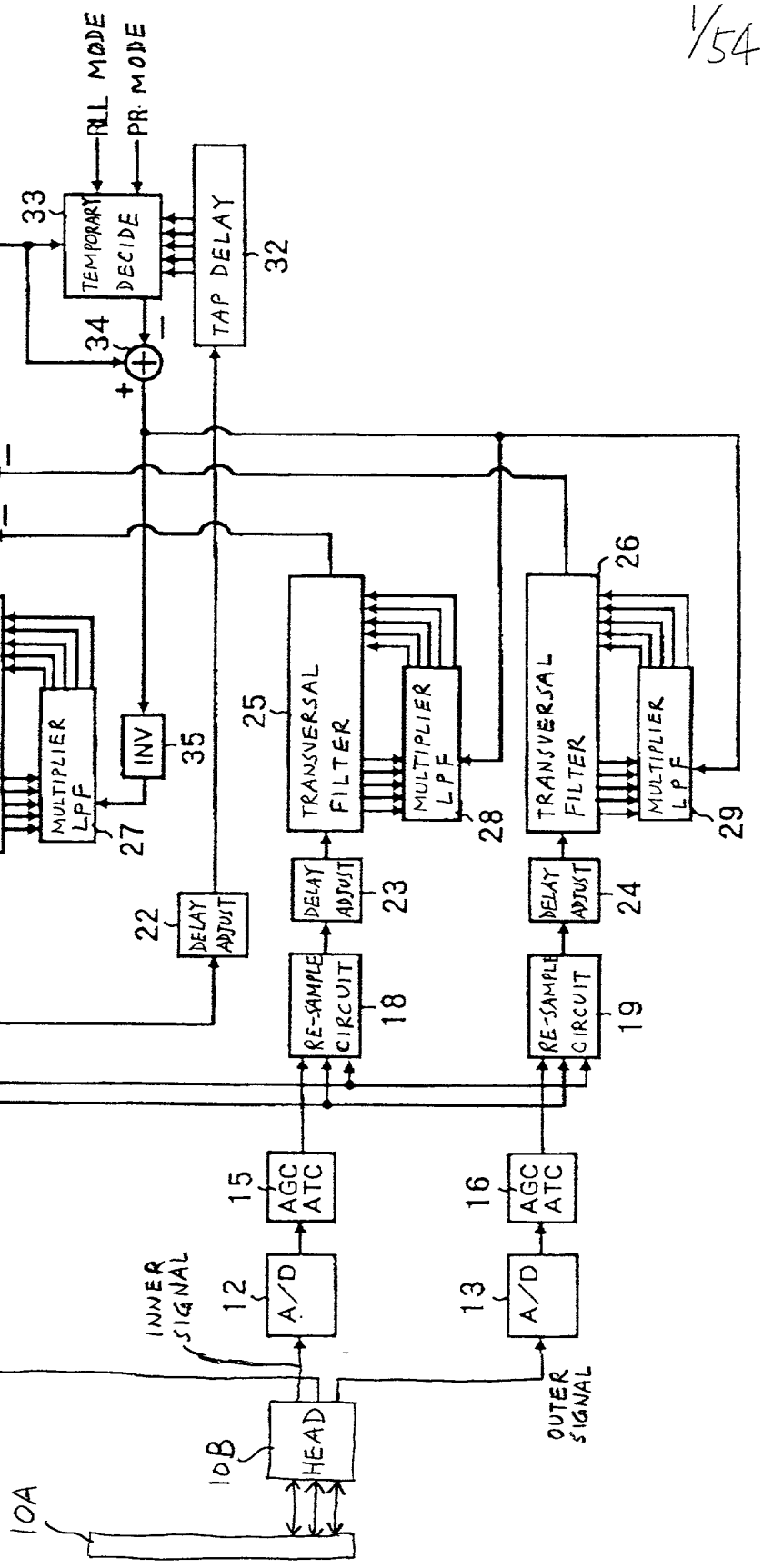

TO VITERBI DECODER
RLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
AGC ATC
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
HEAD
10A
10B
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35

FIG. 2

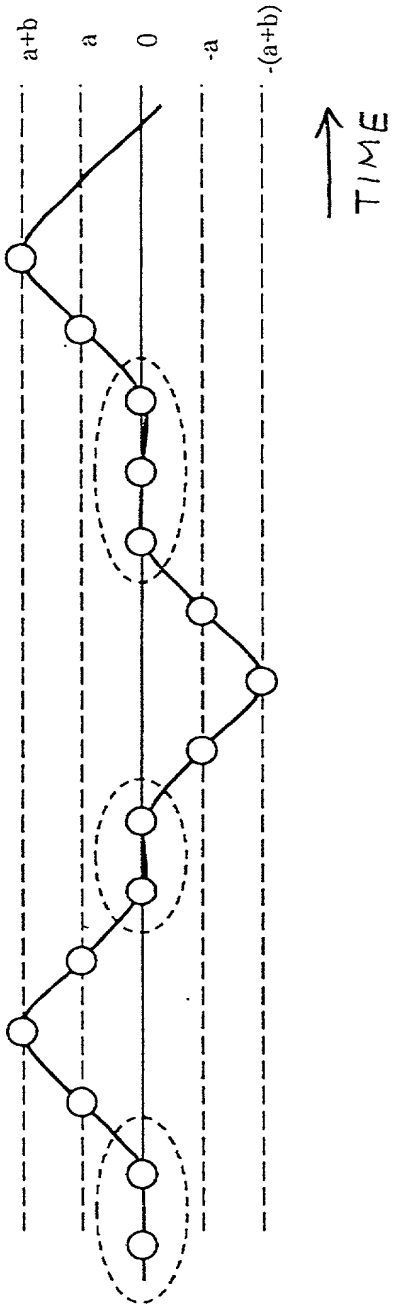


FIG. 3

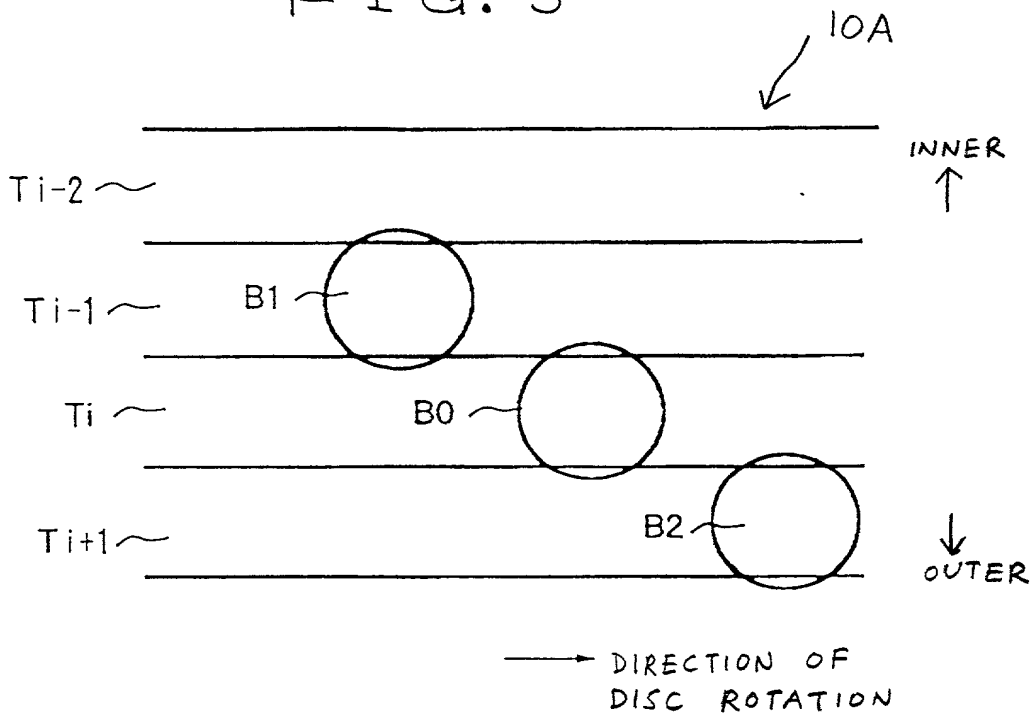

10A
INNER
Ti-2
Ti-1
B1
Ti
B0
Ti+1
B2
OUTER
DIRECTION OF DISC ROTATION

FIG. 4

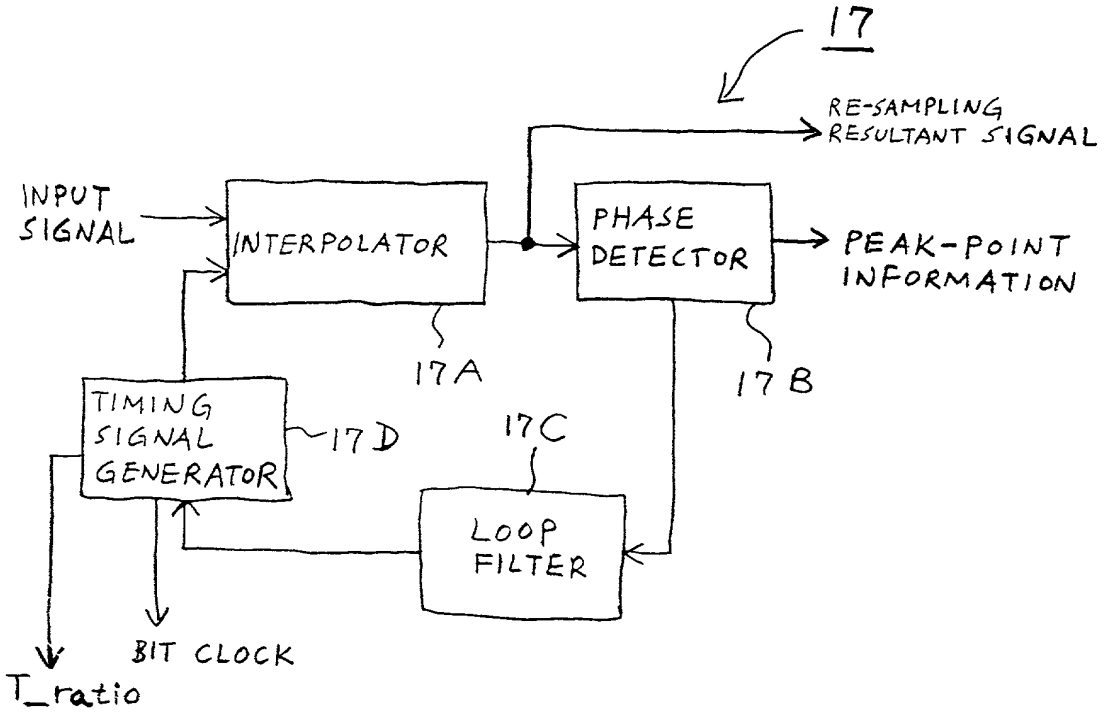

17
RE-SAMPLING RESULTANT SIGNAL
INPUT SIGNAL
INTERPOLATOR
PHASE DETECTOR
PEAK-POINT INFORMATION
17A
17B
TIMING SIGNAL GENERATOR
17D
17C
LOOP FILTER
BIT CLOCK
T_ratio

FIG. 5

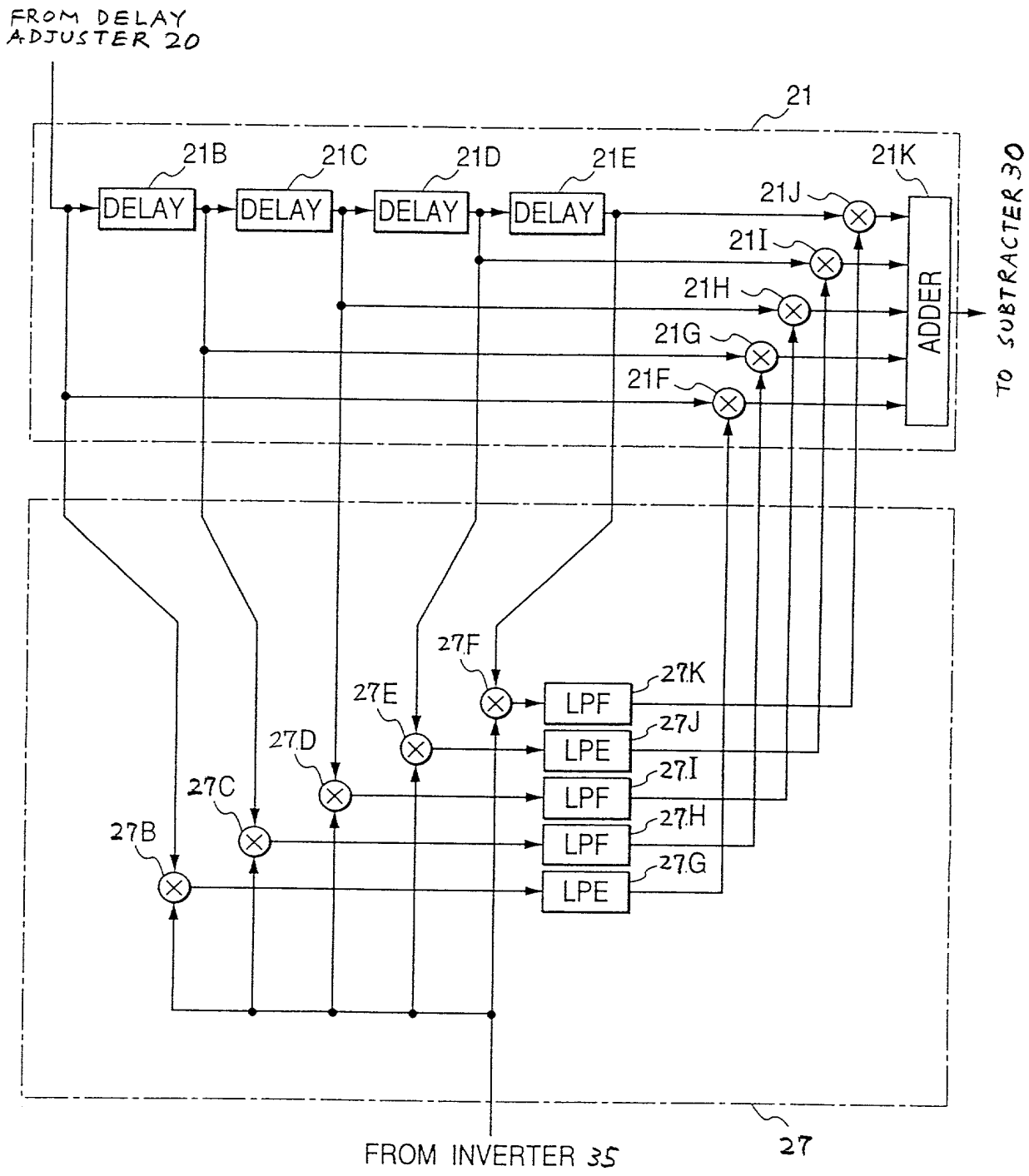

FROM DELAY ADJUSTER 20
21
21B
21C
21D
21E
21K
DELAY
DELAY
DELAY
DELAY
21J
21I
21H
21G
21F
ADDER
TO SUBTRACTER 30
27F
27E
27D
27C
27B
27K
27J
27I
27H
27G
LPF
LPE
LPF
LPF
LPE
FROM INVERTER 35
27

FIG. 6

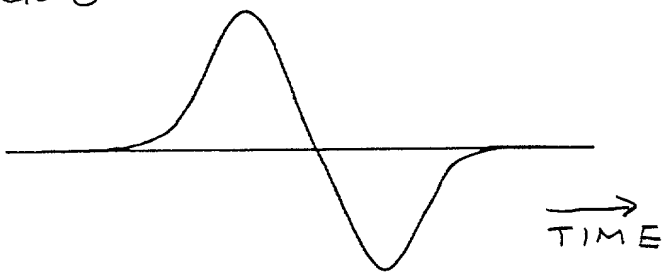


FIG. 7

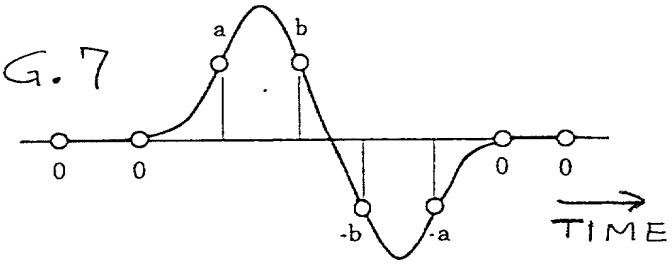
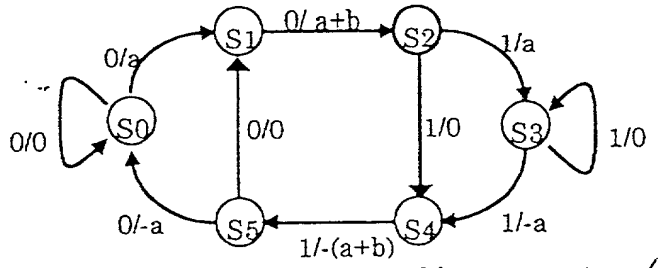
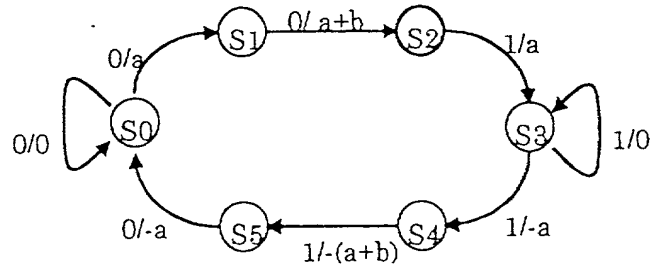


FIG. 8



OUTPUT VALUE/INPUT VALUE

FIG. 9



OUTPUT VALUE/INPUT VALUE

FIG. 10

RLL MODE		RLL(2,X)					
PR MODE		1	2	3	4	5	6
		PR(1, −1)	PR(1,1,−1,−1)	PR(1,2,−2,−1)	PR(1,3,−3,−1)	PR(2,3,−3,−2)	PR(3,4,−4,−3)
TARGET VALUE	a+b	+1	+2	+3	+4	+5	+7
	a	+1	+1	+1	+1	+2	+3
	0	0	0	0	0	0	0
	−a	−1	−1	−1	−1	−2	−3
	−(a+b)	−1	−2	−3	−4	−5	−7
GAIN G		A	A/2	A/3	A/4	A/5	A/7

FIG. 11

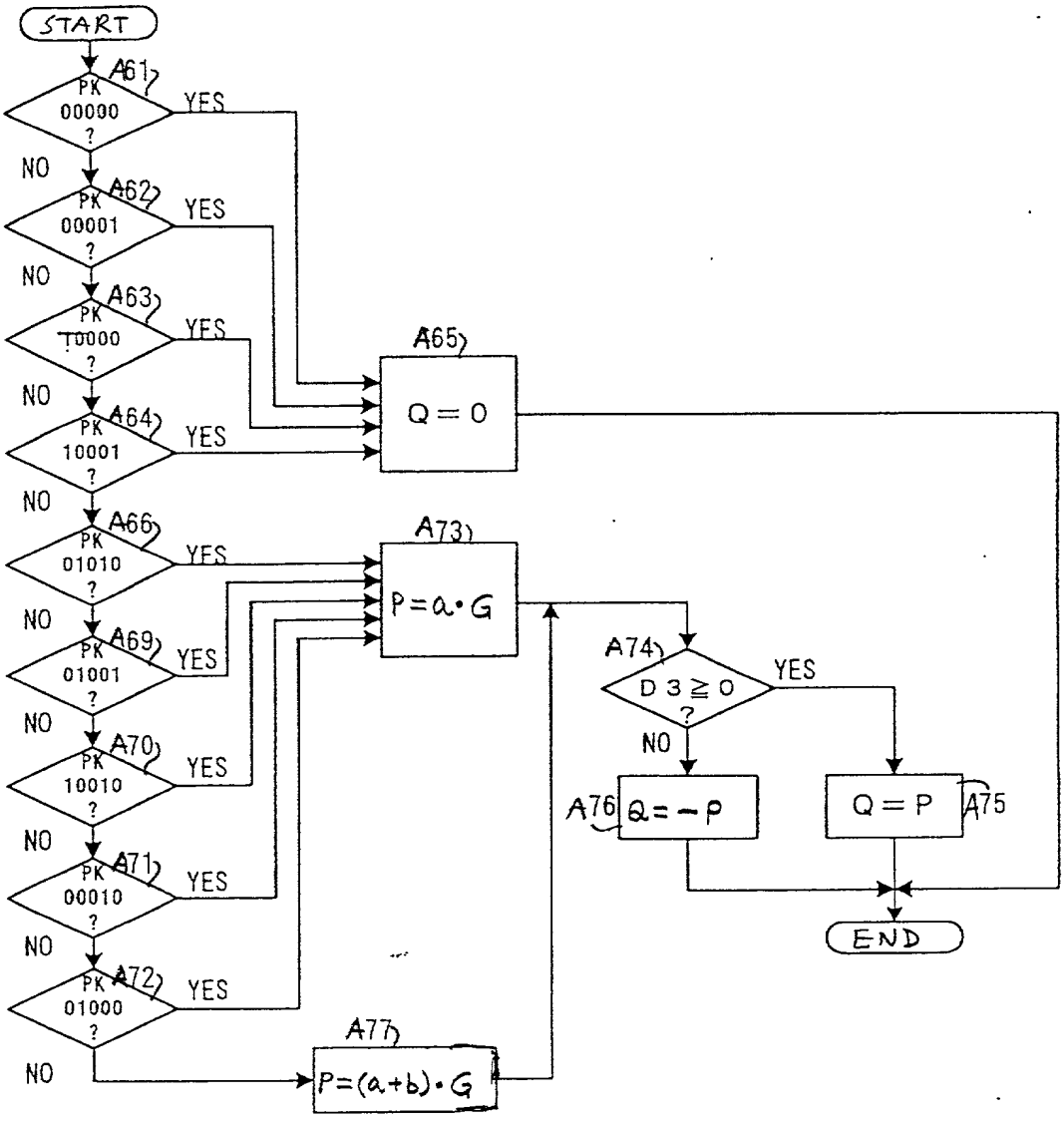

START
A61
PK 00000 ?
YES
NO
A62
PK 00001 ?
YES
NO
A63
PK T0000 ?
YES
NO
A64
PK 10001 ?
YES
NO
A65
Q = 0
A66
PK 01010 ?
YES
NO
A69
PK 01001 ?
YES
NO
A70
PK 10010 ?
YES
NO
A71
PK 00010 ?
YES
NO
A72
PK 01000 ?
YES
NO
A73
P = a · G
A74
D 3 ≧ 0 ?
YES
NO
A75
Q = P
A76
Q = − P
A77
P = (a+b) · G
END

FIG. 12

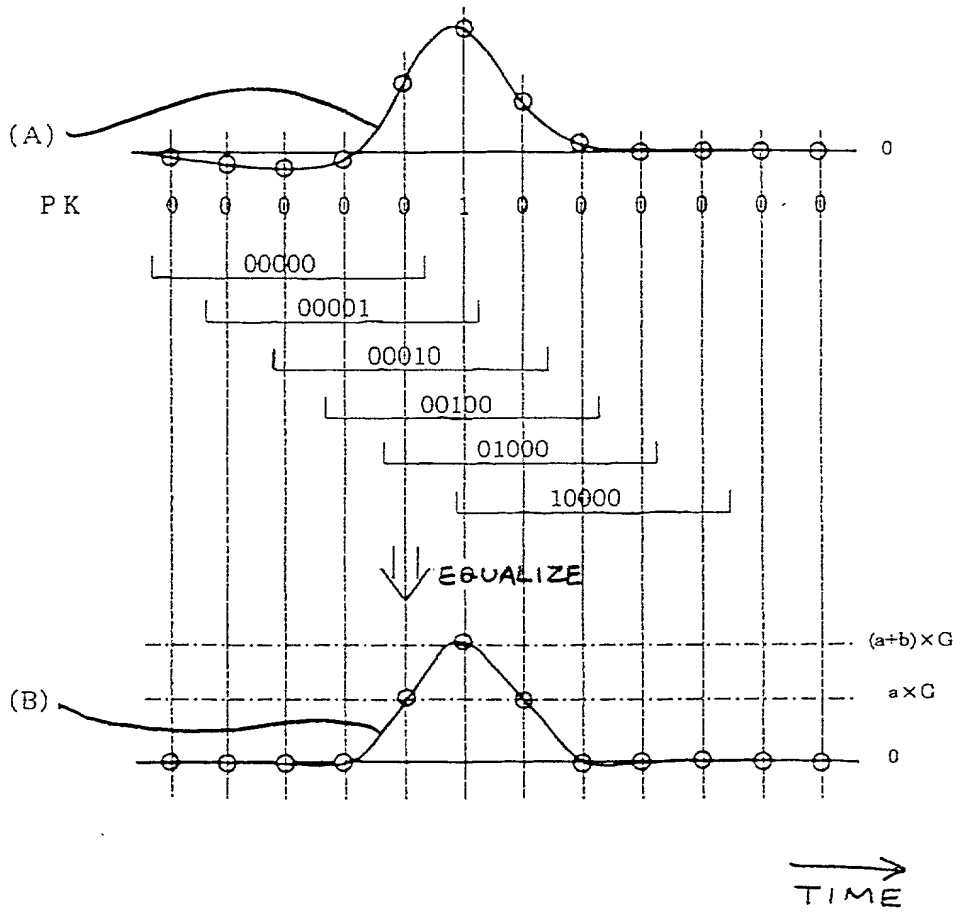

(A)
0
PK
0 0 0 0 0 1 0 0 0 0 0 0
00000
00001
00010
00100
01000
10000
EQUALIZE
(a+b)×G
a×G
(B)
0
TIME

FIG. 13

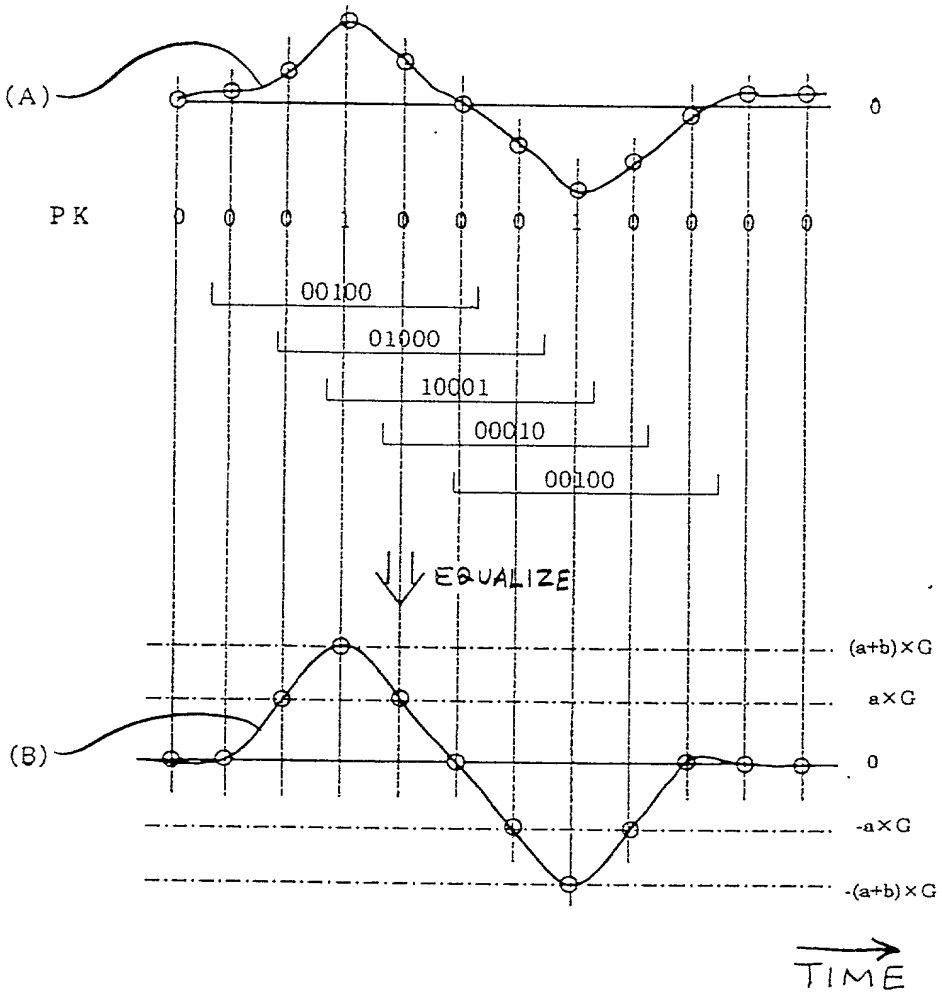

(A)
0
PK
0 0 0 1 0 0 0 1 0 0 0 0
00100
01000
10001
00010
00100
EQUALIZE
(a+b)×G
a×G
(B)
0
-a×G
-(a+b)×G
TIME

FIG. 14

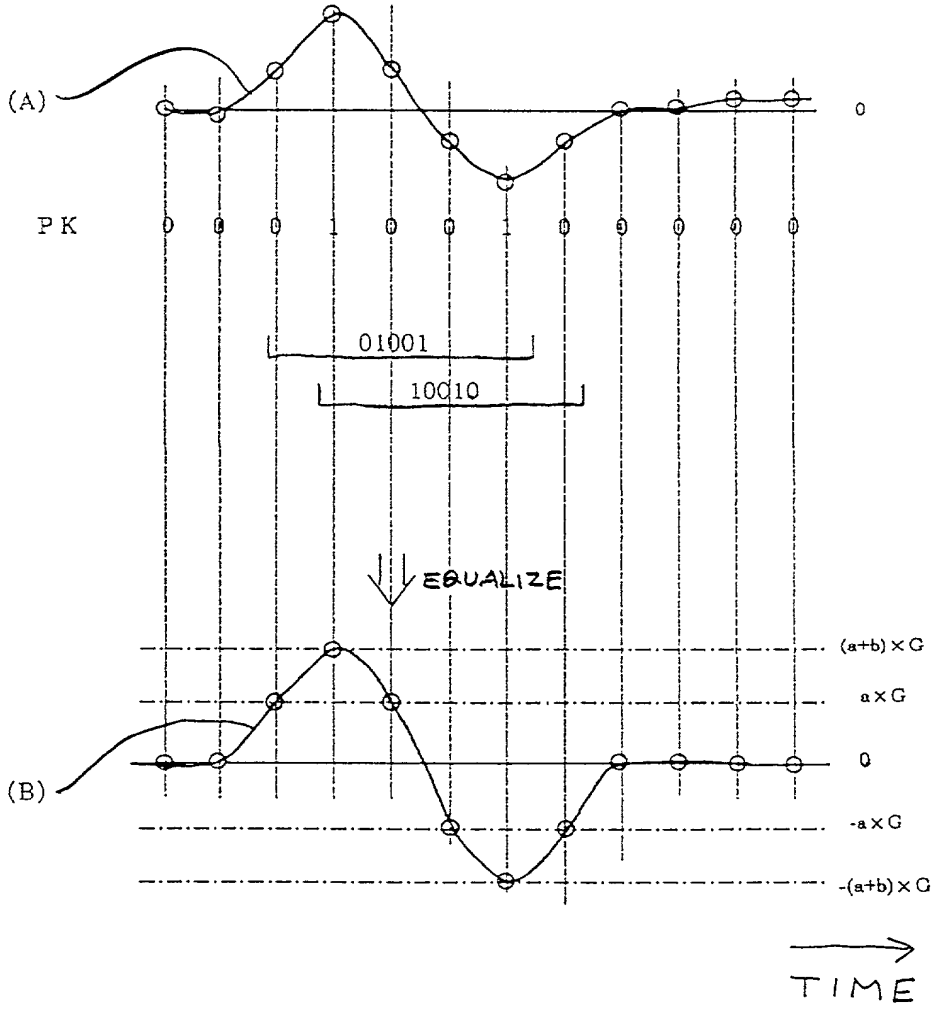
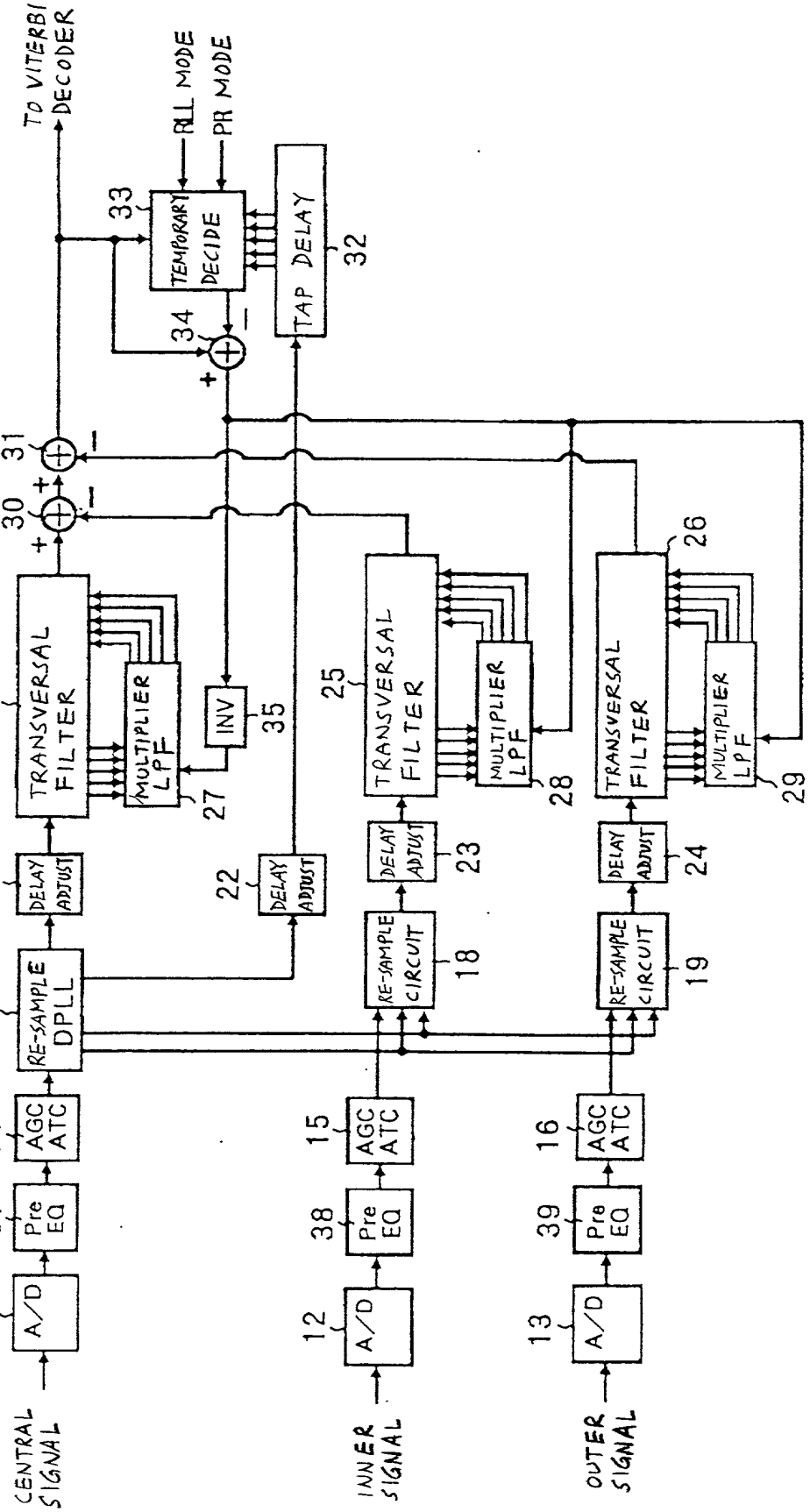

(A)
0
PK
0 0 0 1 0 0 1 0 0 0 0 0
01001
10010
EQUALIZE
(a+b)×G
a×G
0
-a×G
-(a+b)×G
(B)
TIME

FIG. 15


TO VITERBI DECODER
RLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
AGC ATC
Pre EQ
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
11
12
13
14
15
16
17
18
19
20
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23
24
25
26
27
28
29
30
31
32
33
34
35
37
38
39

FIG. 16

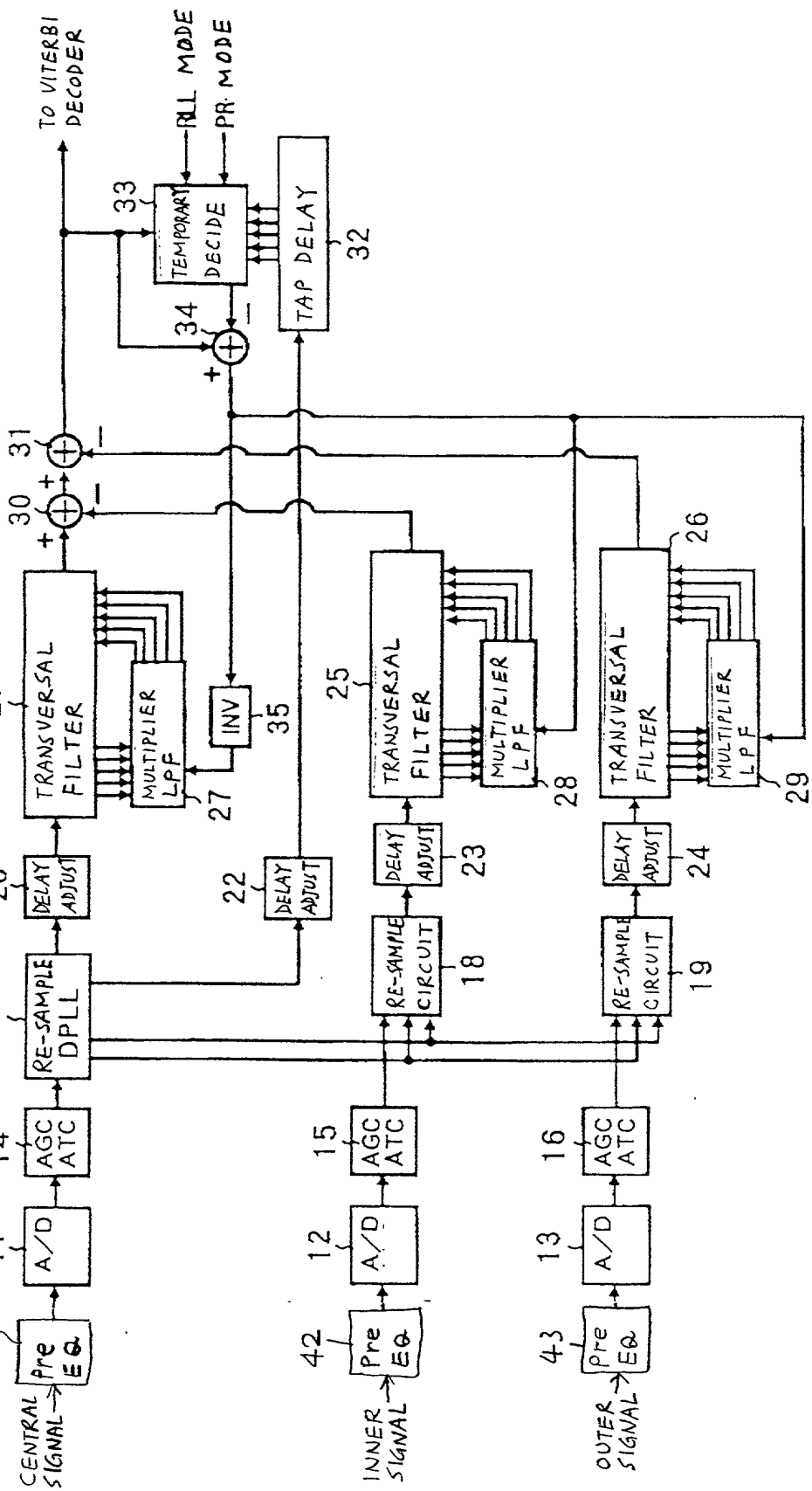
TO VITERBI DECODER
RLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
AGC ATC
A/D
Pre EQ
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
41
42
43

FIG. 17

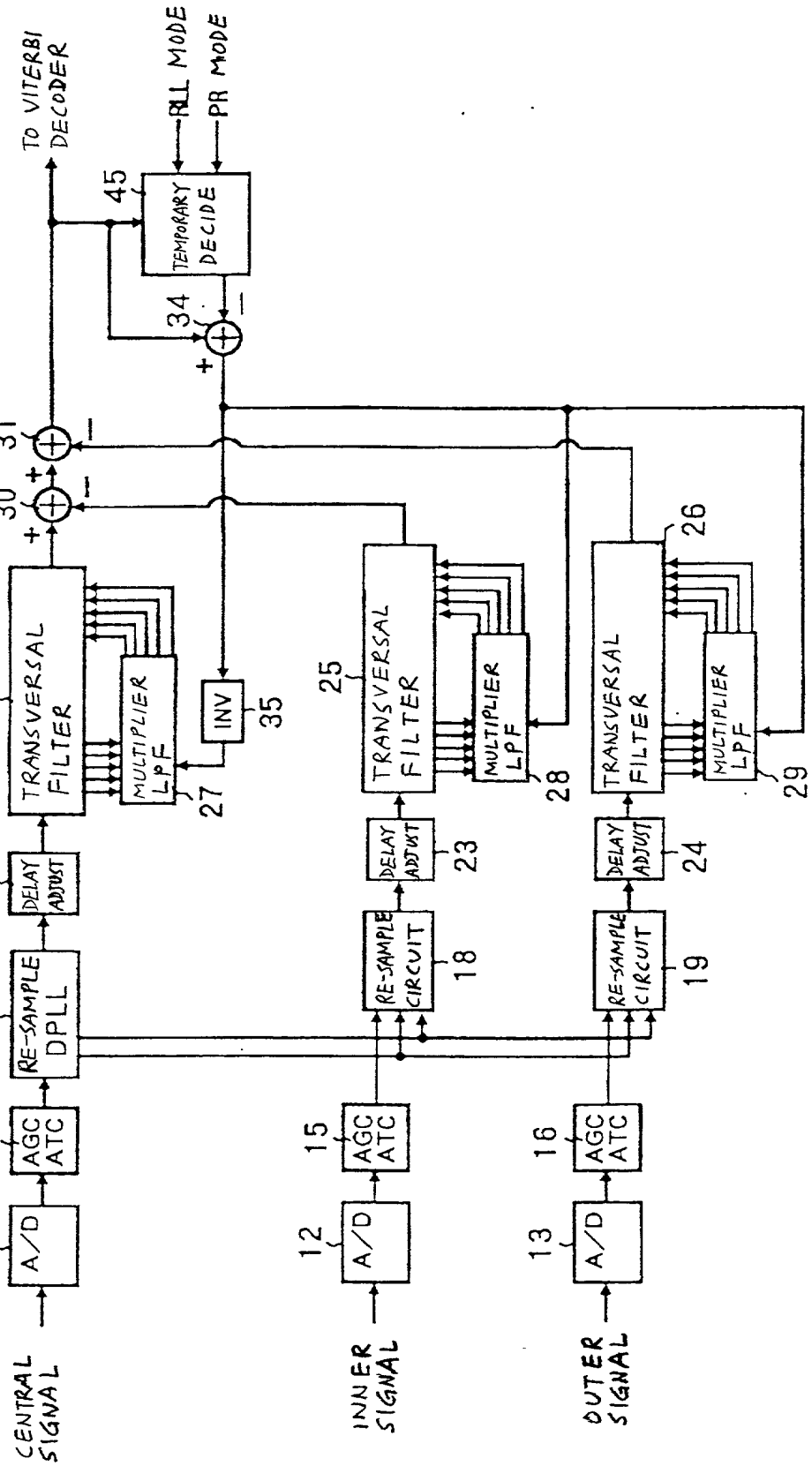
TO VITERBI DECODER
RLL MODE
PR MODE
45
TEMPORARY DECIDE
34
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
20
DELAY ADJUST
17
RE-SAMPLE DPLL
14
AGC ATC
11
A/D
CENTRAL SIGNAL
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
23
DELAY ADJUST
18
RE-SAMPLE CIRCUIT
15
AGC ATC
12
A/D
INNER SIGNAL
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
24
DELAY ADJUST
19
RE-SAMPLE CIRCUIT
16
AGC ATC
13
A/D
OUTER SIGNAL

FIG. 18

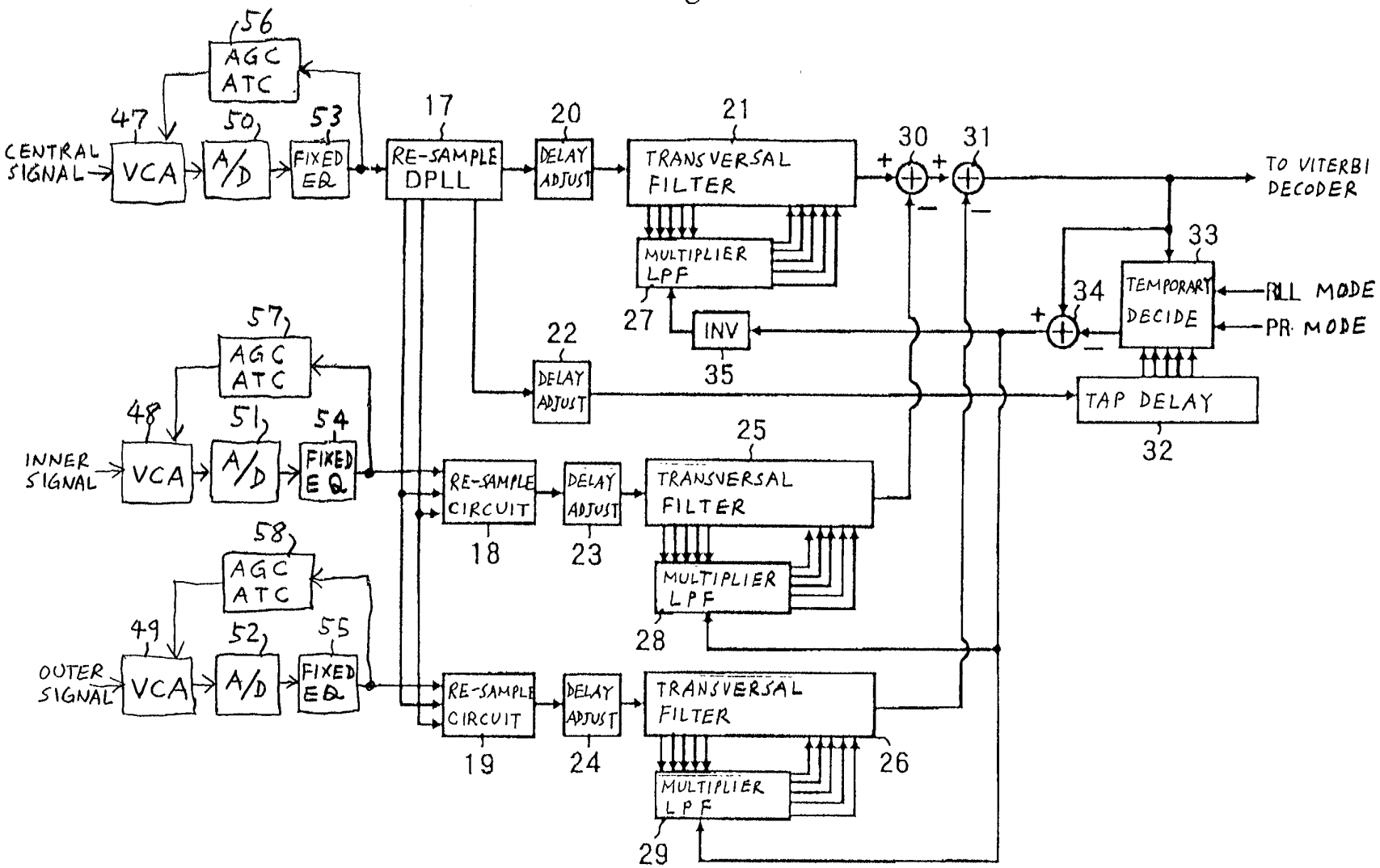
56
AGC ATC
47
50
53
CENTRAL SIGNAL
VCA
A/D
FIXED EQ
17
RE-SAMPLE DPLL
20
DELAY ADJUST
21
TRANSVERSAL FILTER
30
31
TO VITERBI DECODER
MULTIPLIER LPF
27
INV
35
33
TEMPORARY DECIDE
34
PLL MODE
PR MODE
57
AGC ATC
22
DELAY ADJUST
TAP DELAY
32
48
51
54
INNER SIGNAL
VCA
A/D
FIXED EQ
25
RE-SAMPLE CIRCUIT
18
DELAY ADJUST
23
TRANSVERSAL FILTER
MULTIPLIER LPF
28
58
AGC ATC
49
52
55
OUTER SIGNAL
VCA
A/D
FIXED EQ
RE-SAMPLE CIRCUIT
19
DELAY ADJUST
24
TRANSVERSAL FILTER
26
MULTIPLIER LPF
29

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FIG. 19

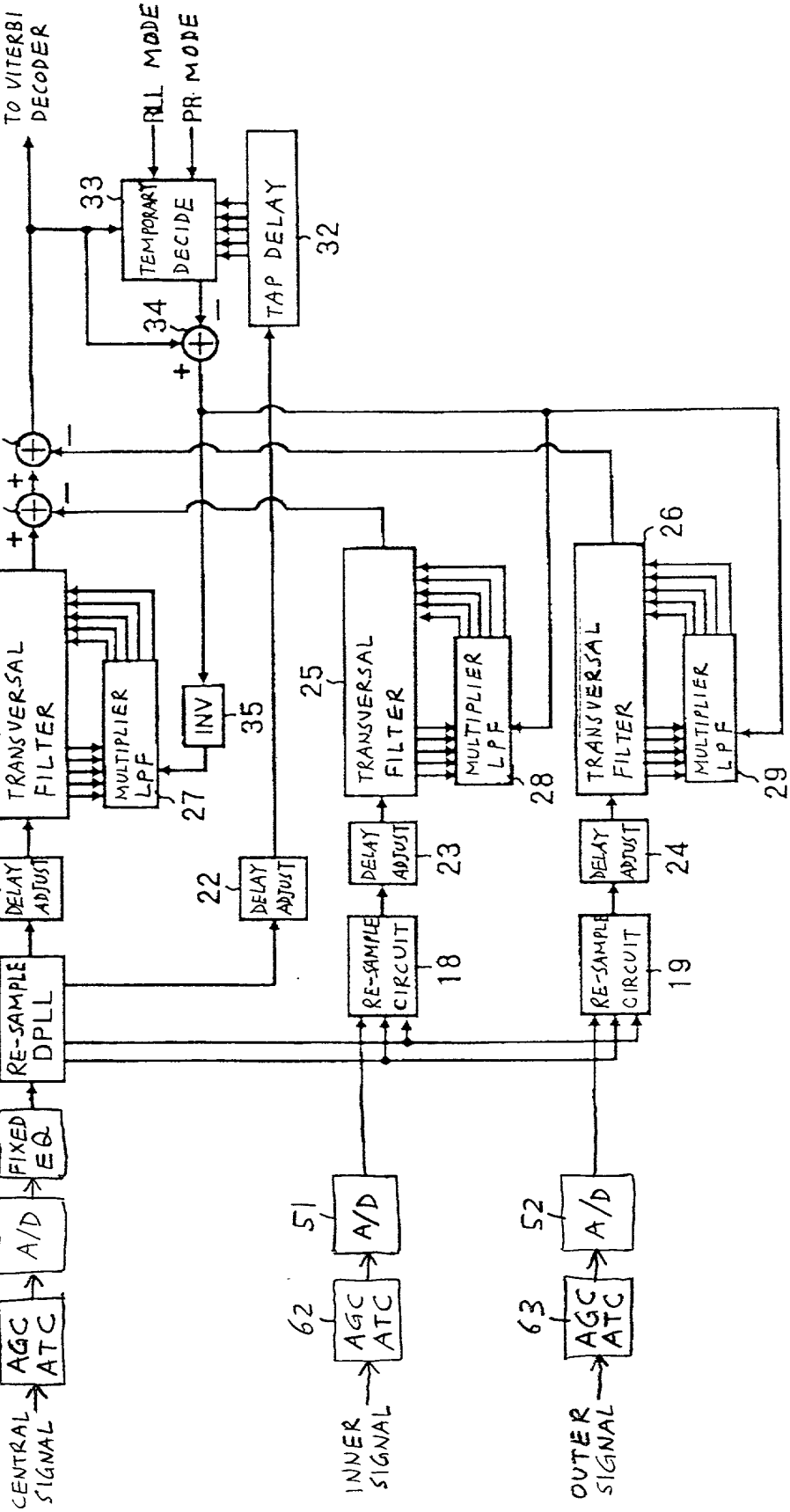
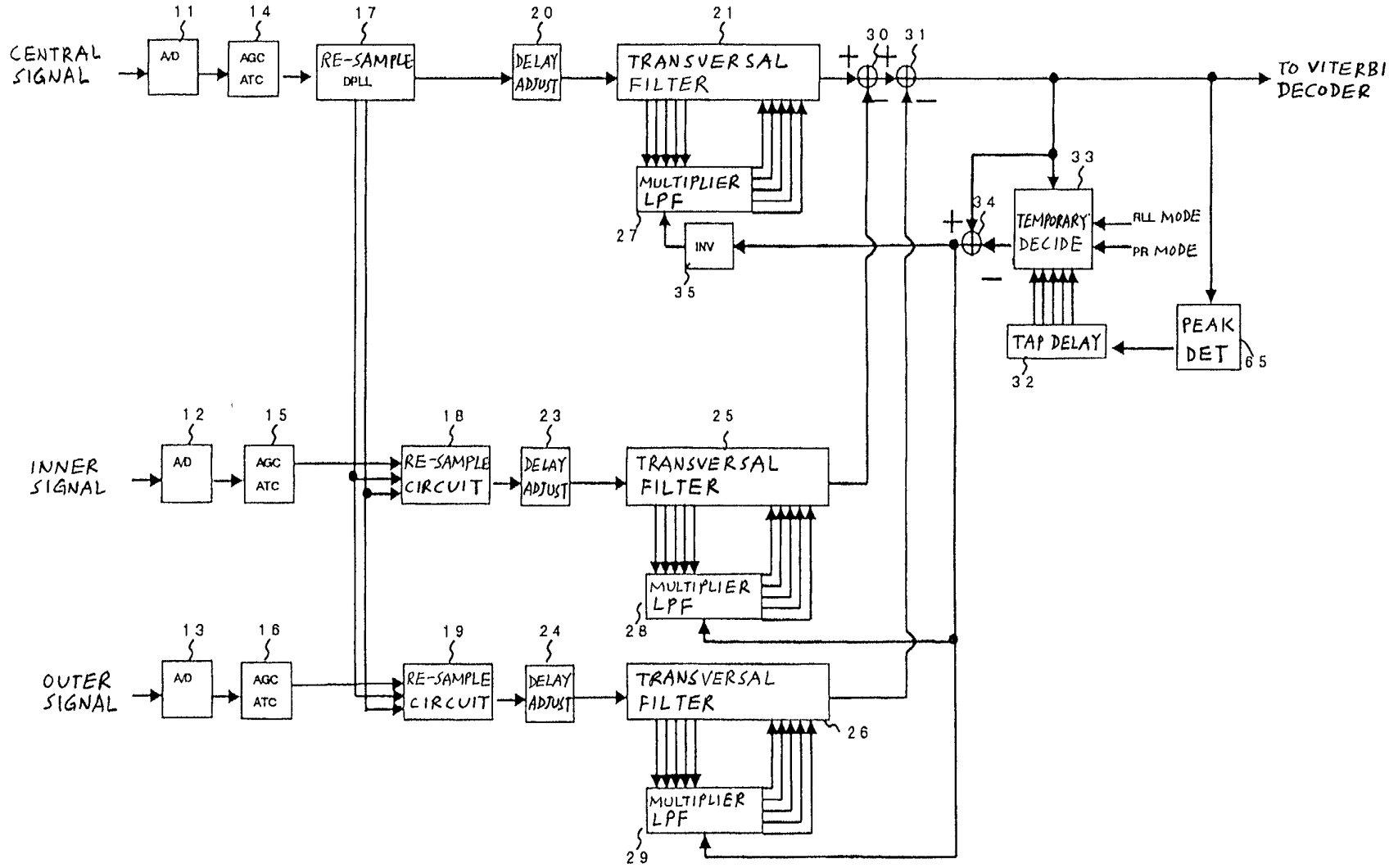

TO VITERBI DECODER
PLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
FIXED EQ
A/D
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
21
20
22
25
23
27
28
26
24
29
30
31
33
34
35
17
18
19
53
50
51
52
61
62
63

FIG. 20


CENTRAL SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
DELAY ADJUST
TRANSVERSAL FILTER
TO VITERBI DECODER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
RLL MODE
PR MODE
TAP DELAY
PEAK DET
INNER SIGNAL
RE-SAMPLE CIRCUIT
OUTER SIGNAL
11
12
13
14
15
16
17
18
19
20
21
23
24
25
26
27
28
29
30
31
32
33
34
35
65

h-5/91

FIG. 21

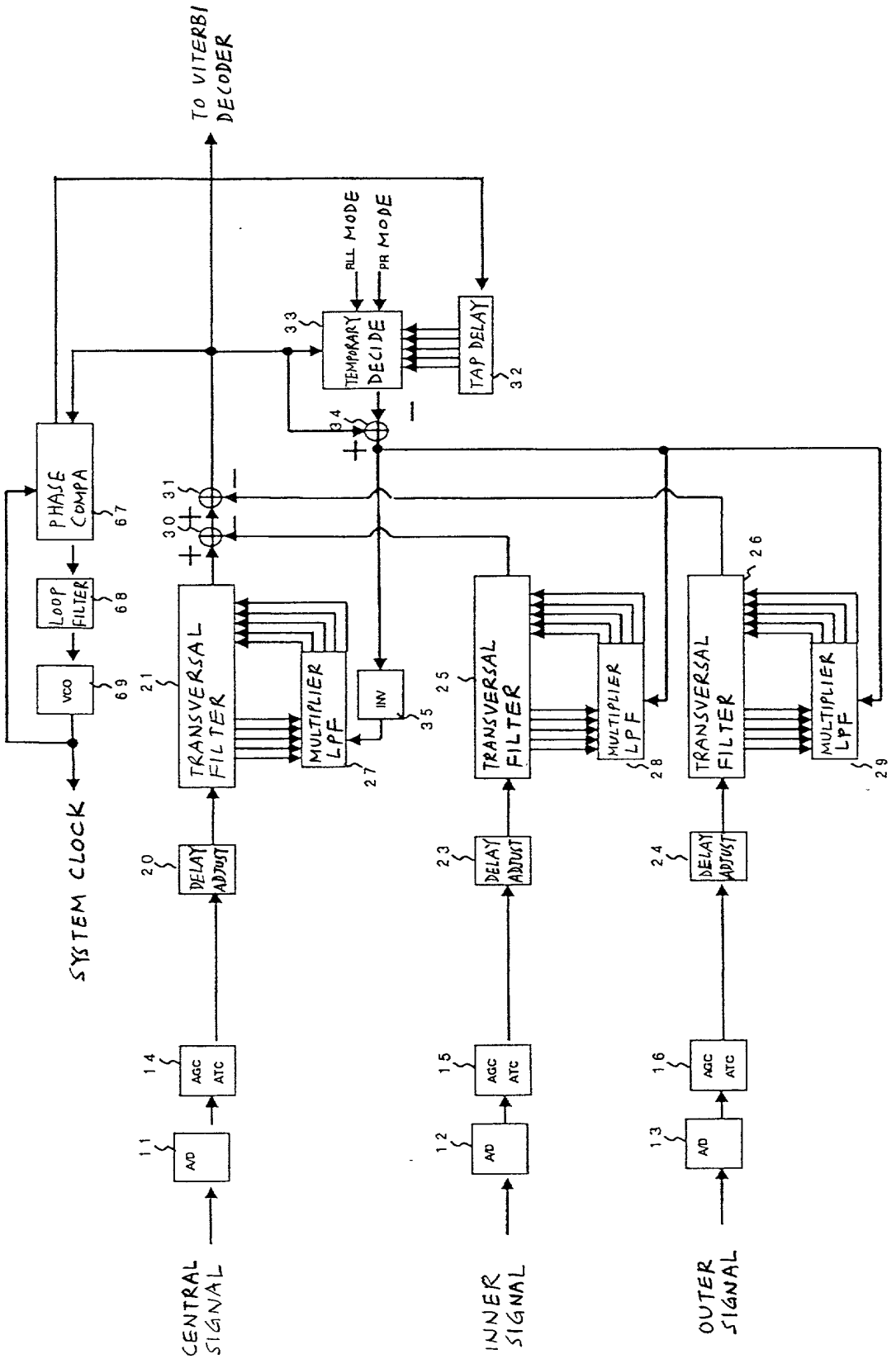

TO VITERBI DECODER
RLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
PHASE COMPA
LOOP FILTER
VCO
SYSTEM CLOCK
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
AGC ATC
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 22

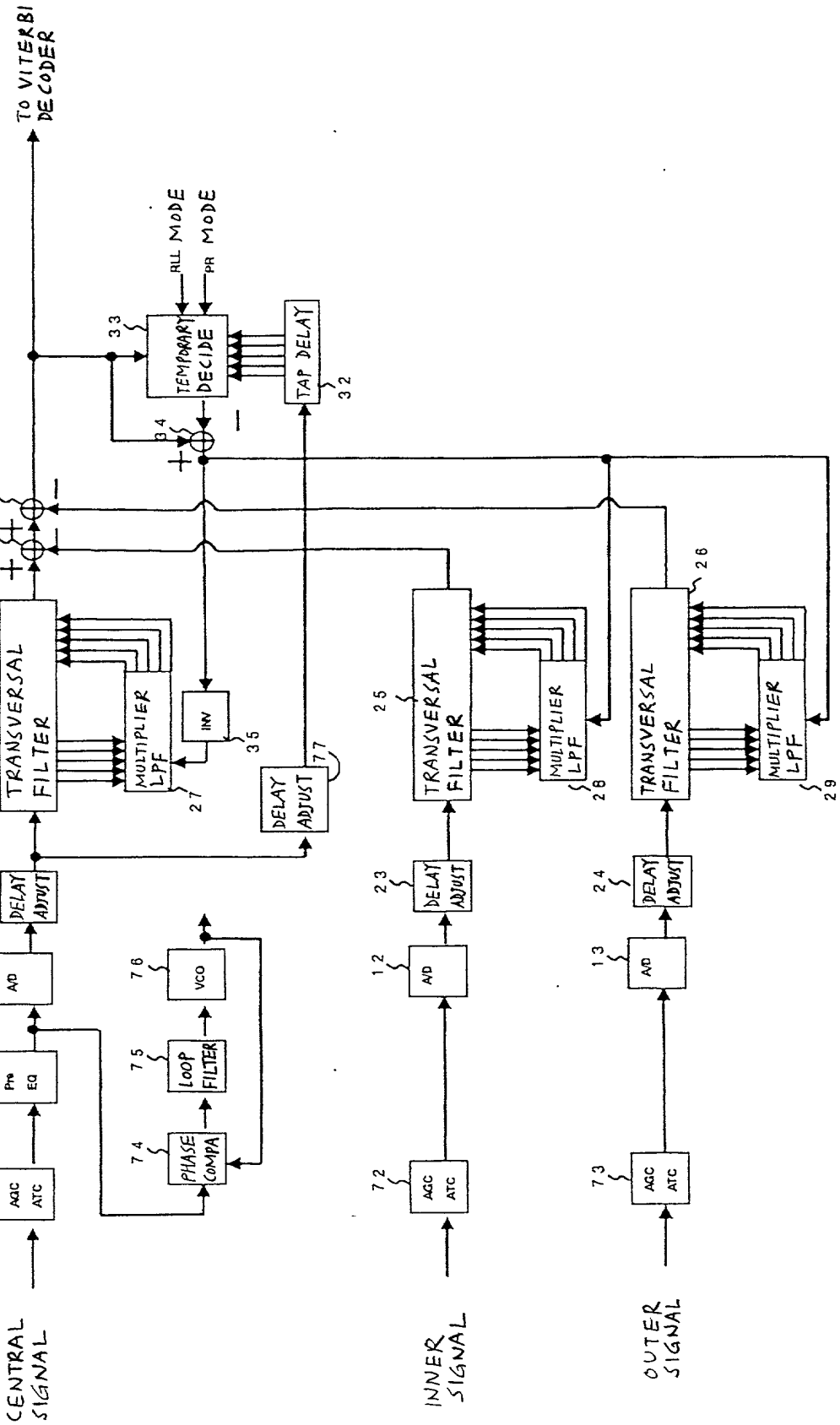

TO VITERBI DECODER
RLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
AGC ATC
Pre EQ
A/D
VCO
LOOP FILTER
PHASE COMPA
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 23

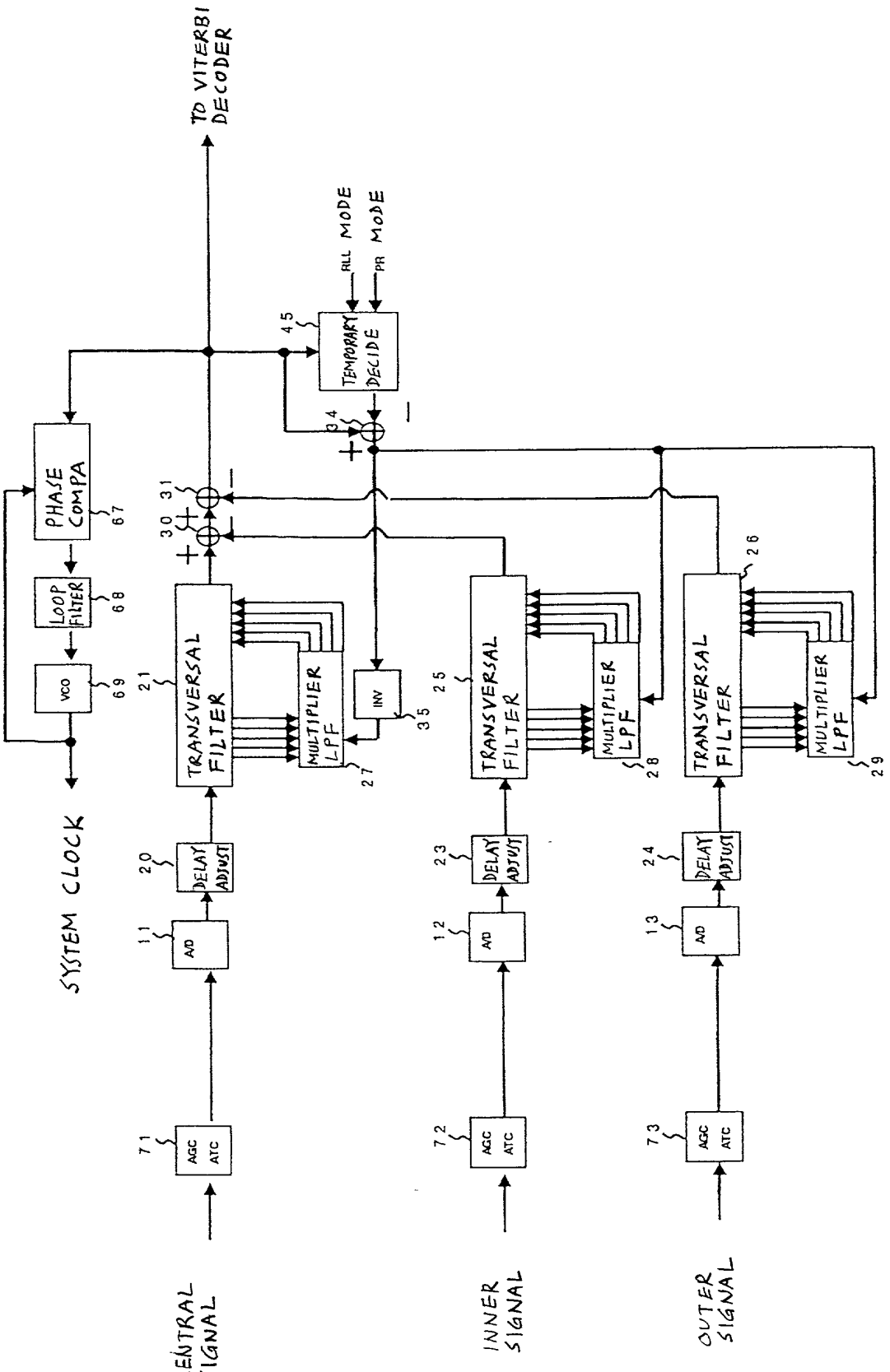

TO VITERBI DECODER
SYSTEM CLOCK
PHASE COMPA
LOOP FILTER
VCO
TEMPORARY DECIDE
ALL MODE
PR MODE
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
A/D
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 24

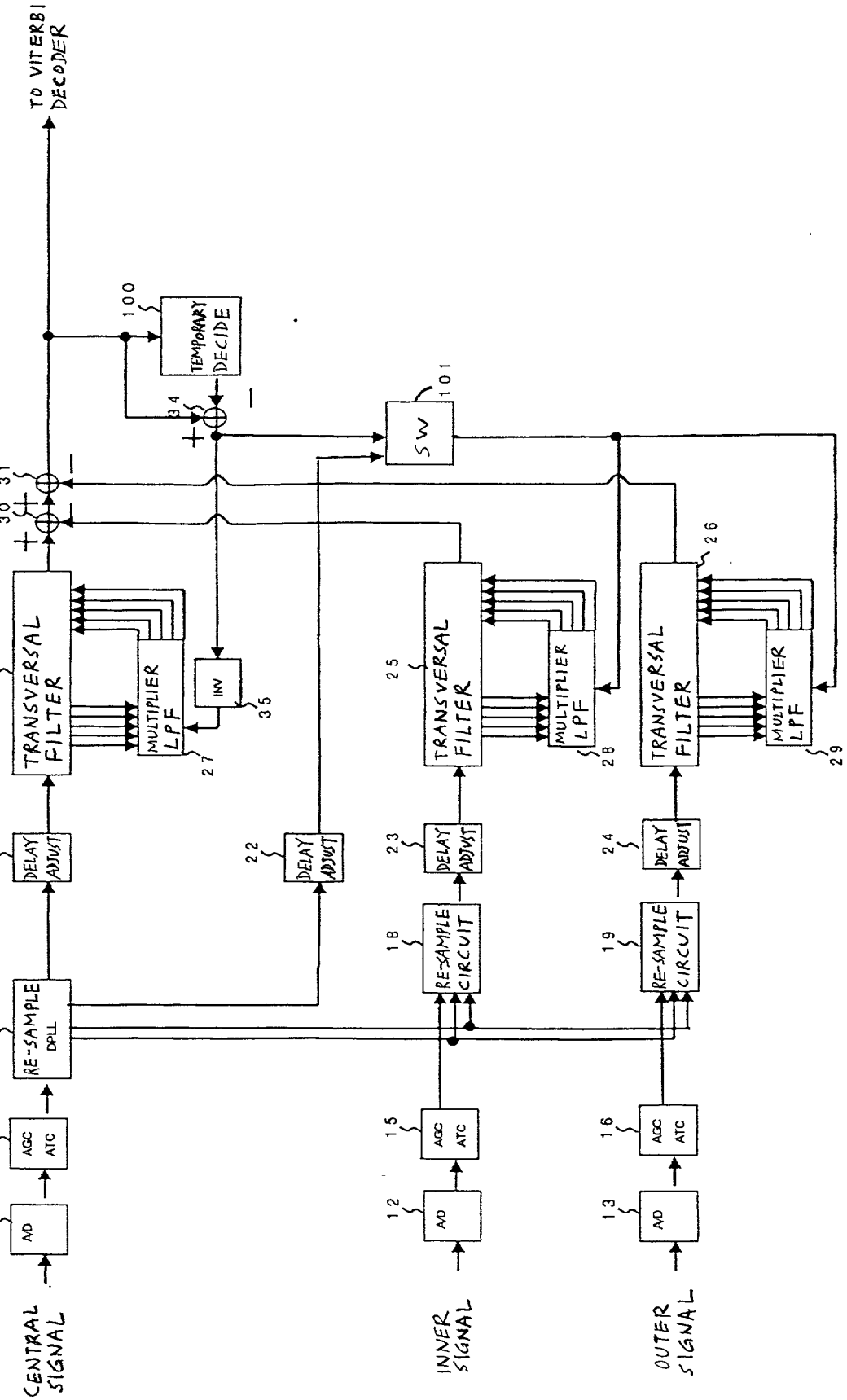

TO VITERBI DECODER
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
SW
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
34
35
100
101

FIG. 25

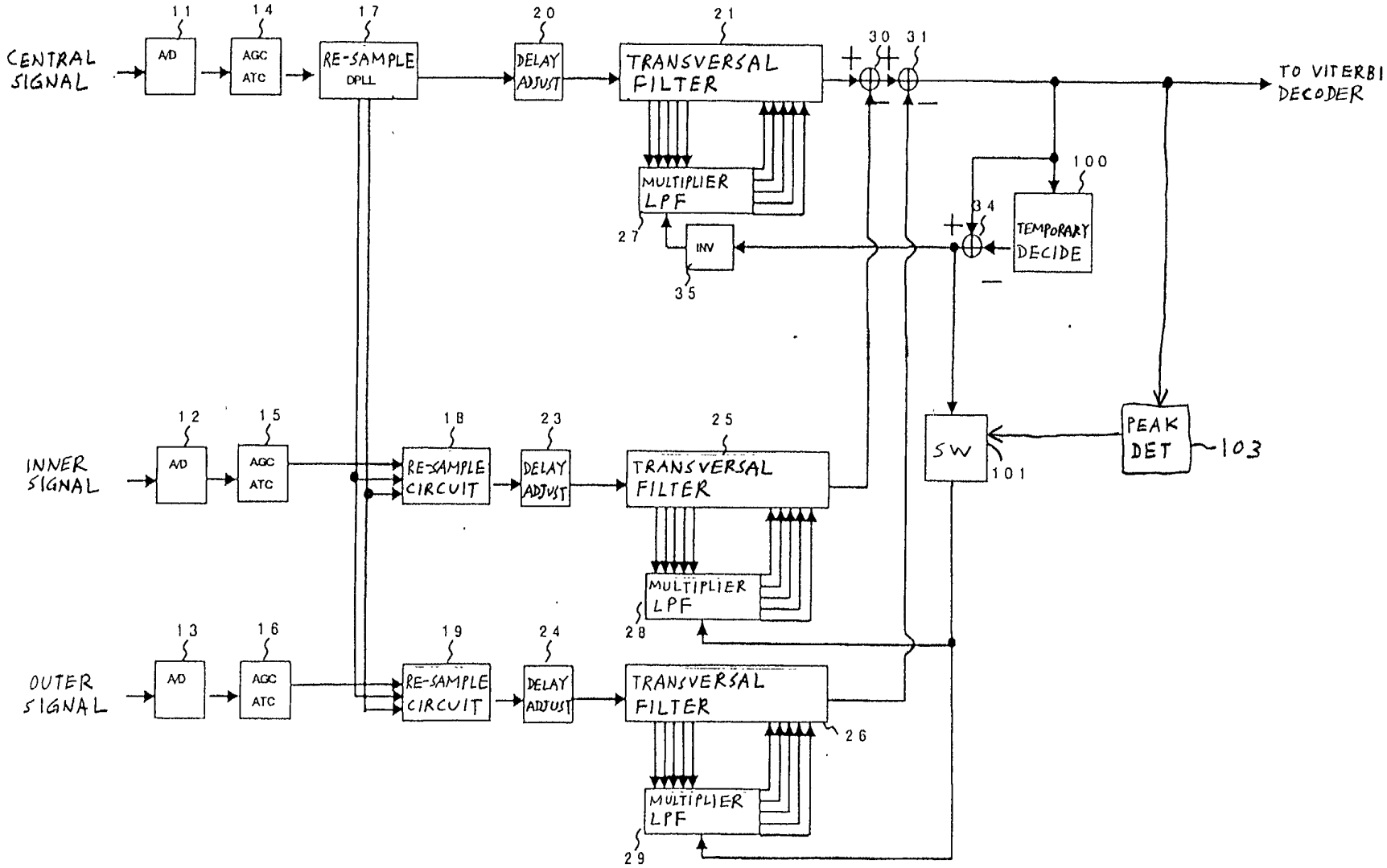

CENTRAL SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
TO VITERBI DECODER
INNER SIGNAL
RE-SAMPLE CIRCUIT
OUTER SIGNAL
SW
PEAK DET
11
12
13
14
15
16
17
18
19
20
21
23
24
25
26
27
28
29
30
31
34
35
100
101
103

FIG. 26

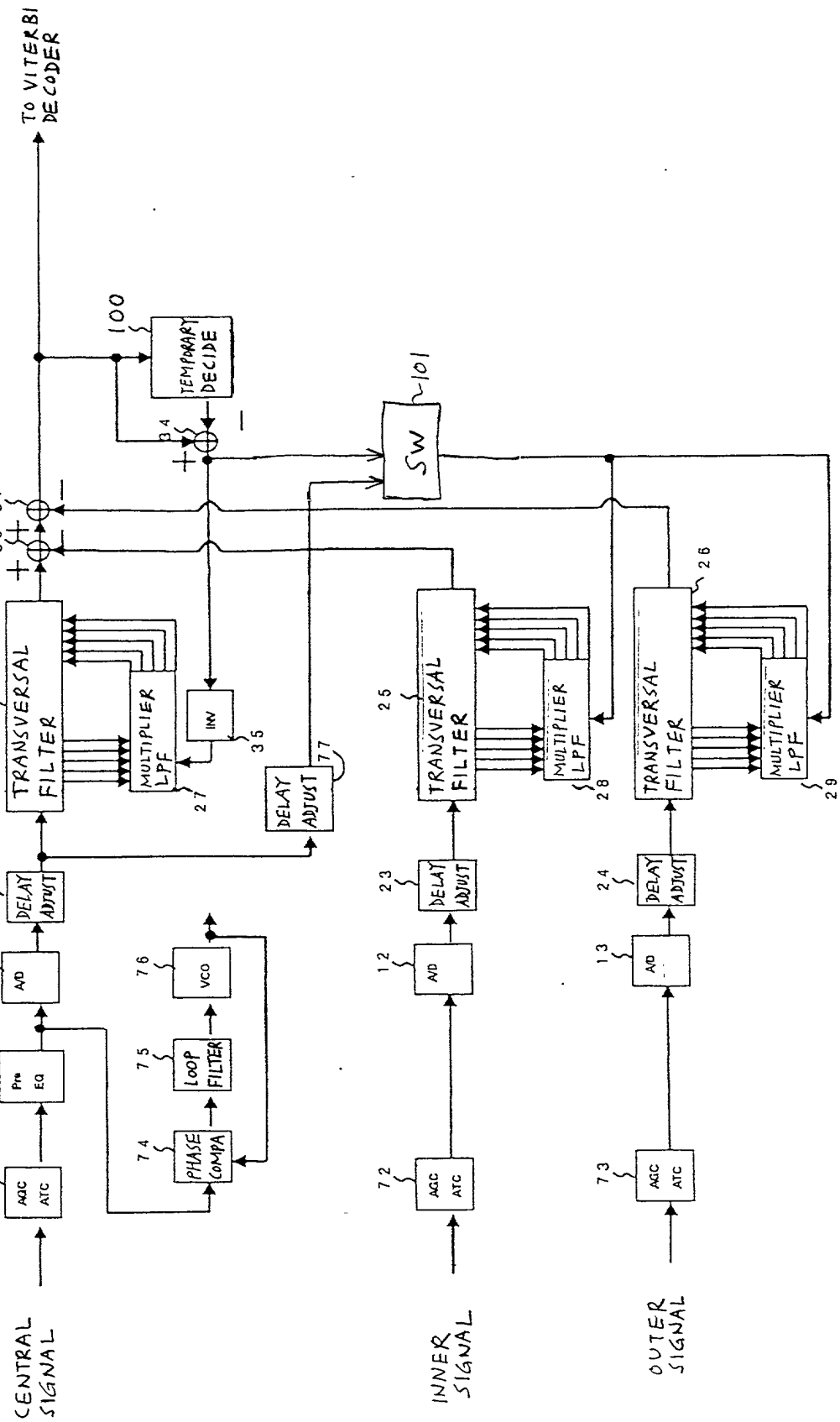

TO VITERBI DECODER
100
TEMPORARY DECIDE
101
SW
34
30
31
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
DELAY ADJUST
77
20
DELAY ADJUST
11
A/D
41
Pre EQ
71
AGC ATC
CENTRAL SIGNAL
74
PHASE COMPA
75
LOOP FILTER
76
VCO
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
23
DELAY ADJUST
12
A/D
72
AGC ATC
INNER SIGNAL
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
24
DELAY ADJUST
13
A/D
73
AGC ATC
OUTER SIGNAL

FIG. 27

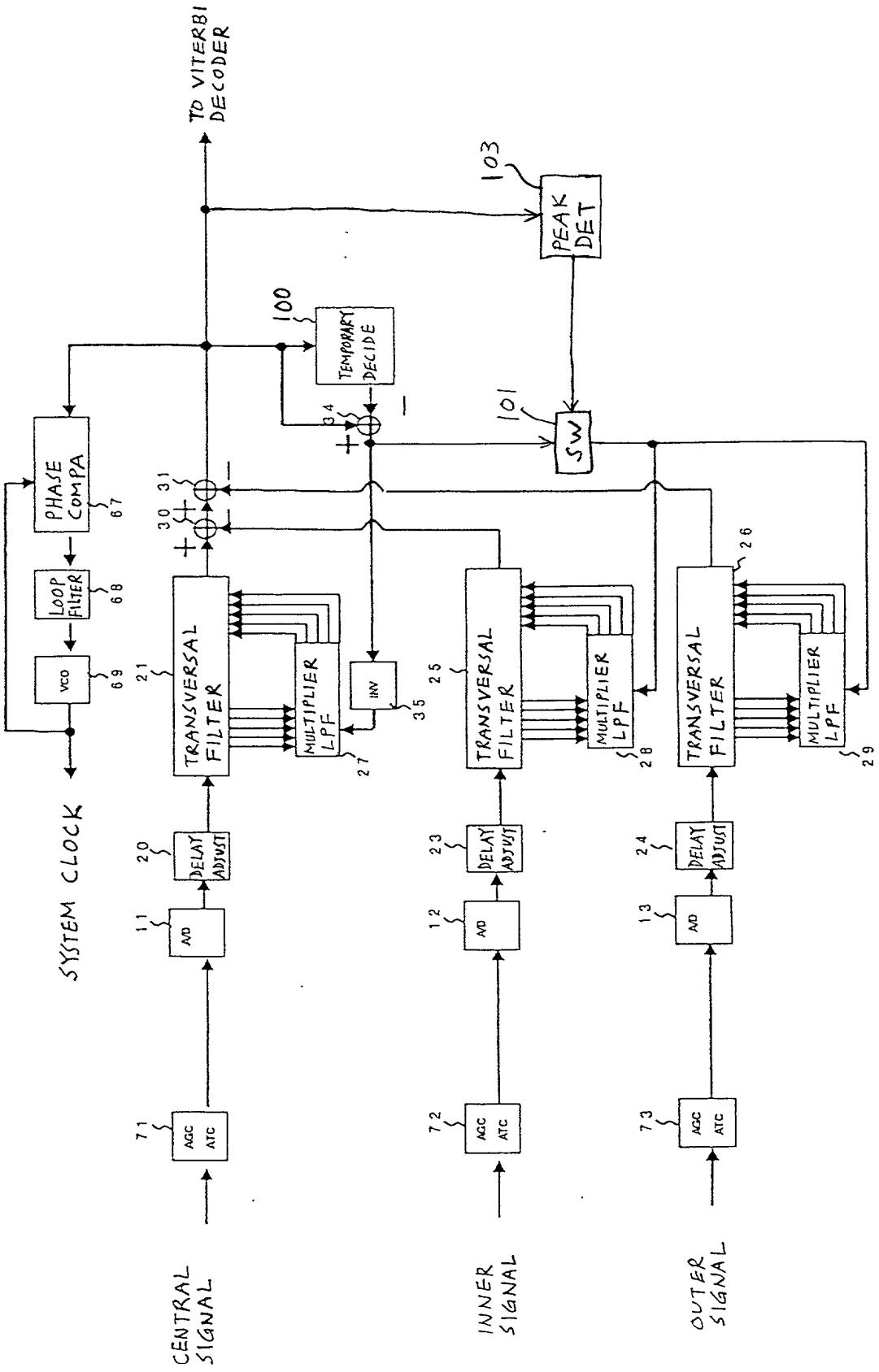

TO VITERBI DECODER
SYSTEM CLOCK
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
AGC ATC
A/D
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
PEAK DET
SW
PHASE COMPA
LOOP FILTER
VCO
100
101
103
11
12
13
20
21
23
24
25
26
27
28
29
30
31
34
35
67
68
69
71
72
73

FIG. 28

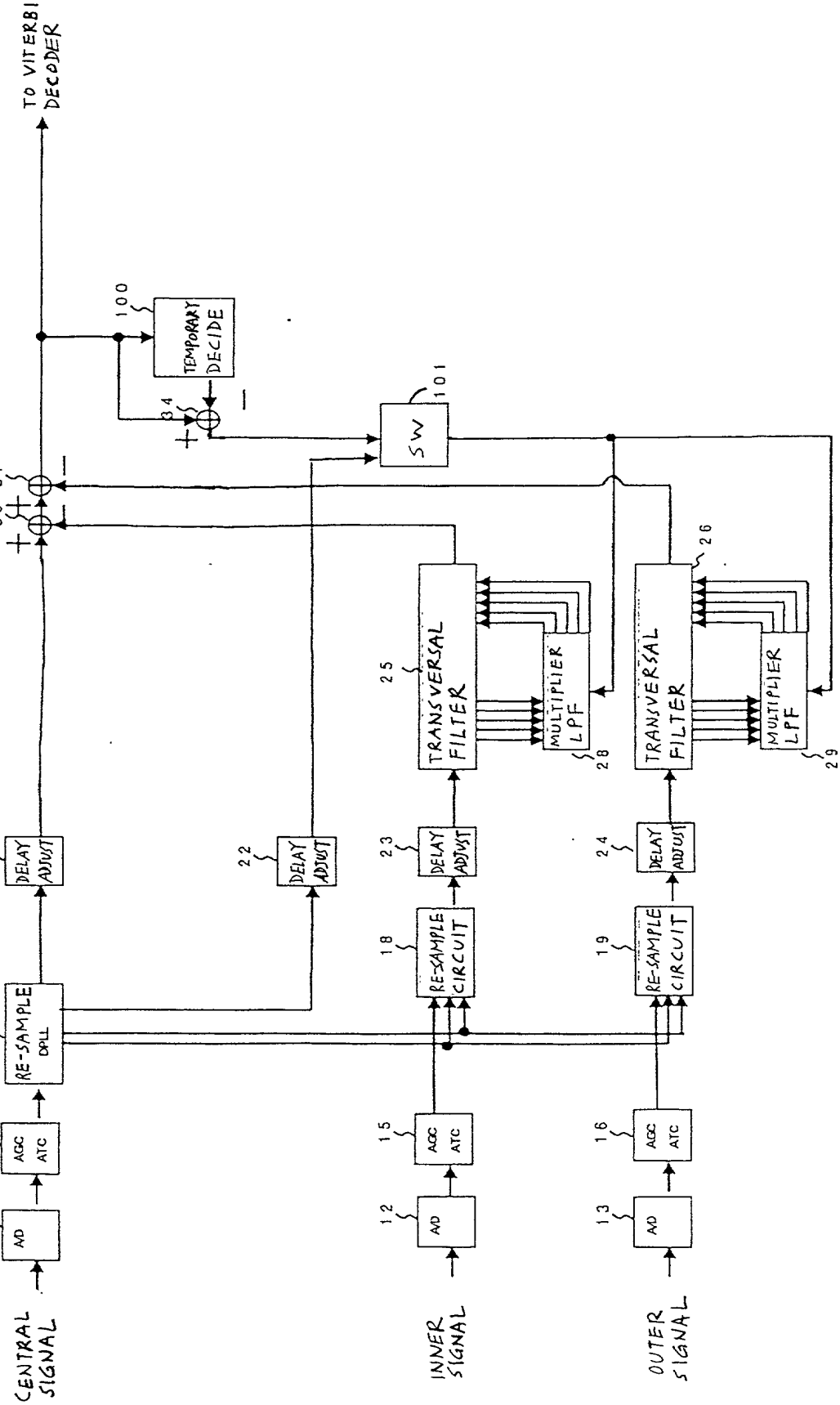

TO VITERBI DECODER
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
DELAY ADJUST
RE-SAMPLE CIRCUIT
TRANSVERSAL FILTER
MULTIPLIER LPF
TEMPORARY DECIDE
SW
11
12
13
14
15
16
17
18
19
20
22
23
24
25
26
28
29
30
31
34
100
101

FIG. 29

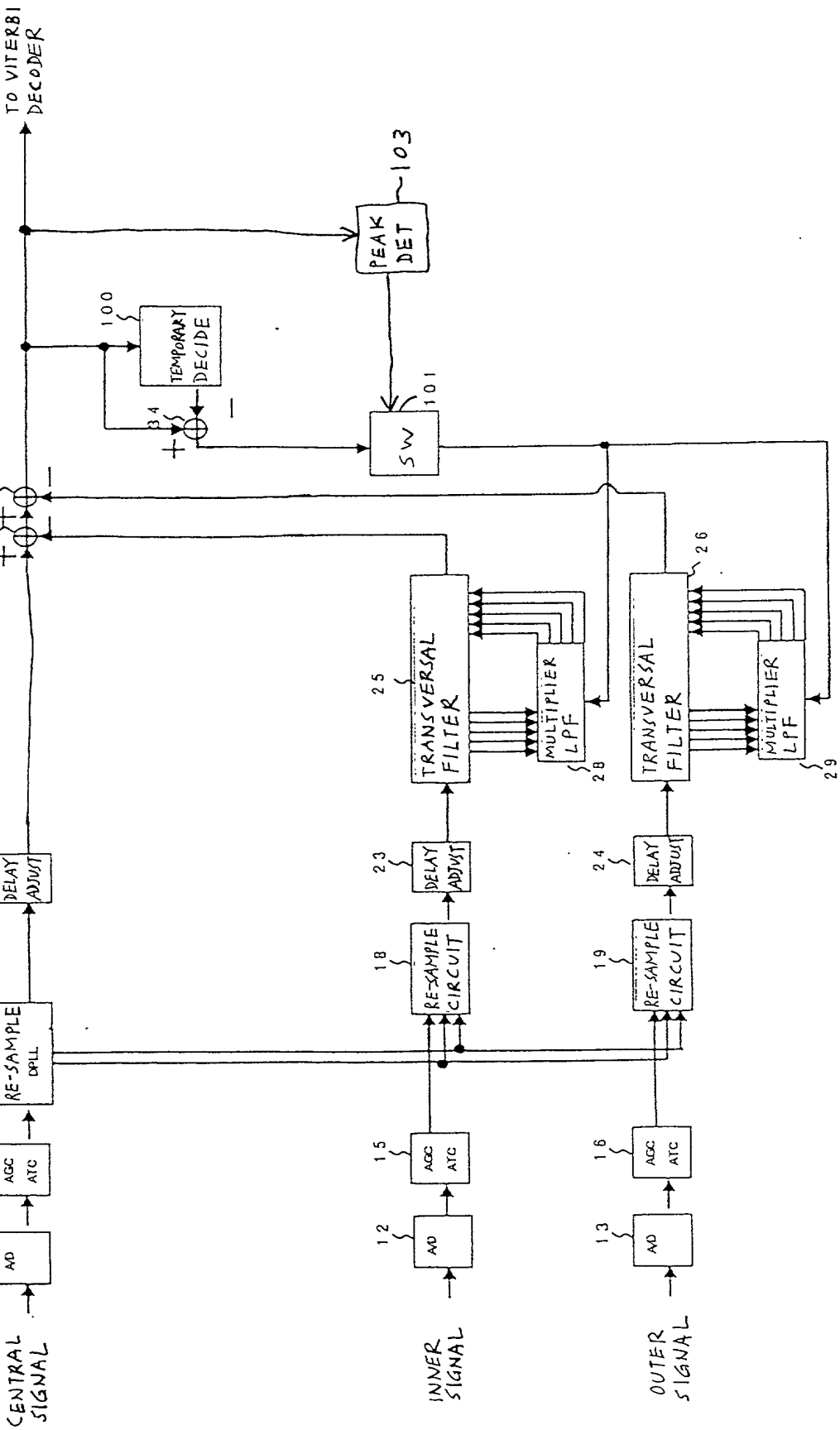

TO VITERBI DECODER
PEAK DET
103
100
TEMPORARY DECIDE
SW
101
34
30
31
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
DELAY ADJUST
RE-SAMPLE CIRCUIT
TRANSVERSAL FILTER
MULTIPLIER LPF
11
12
13
14
15
16
17
18
19
20
23
24
25
26
28
29

FIG. 30

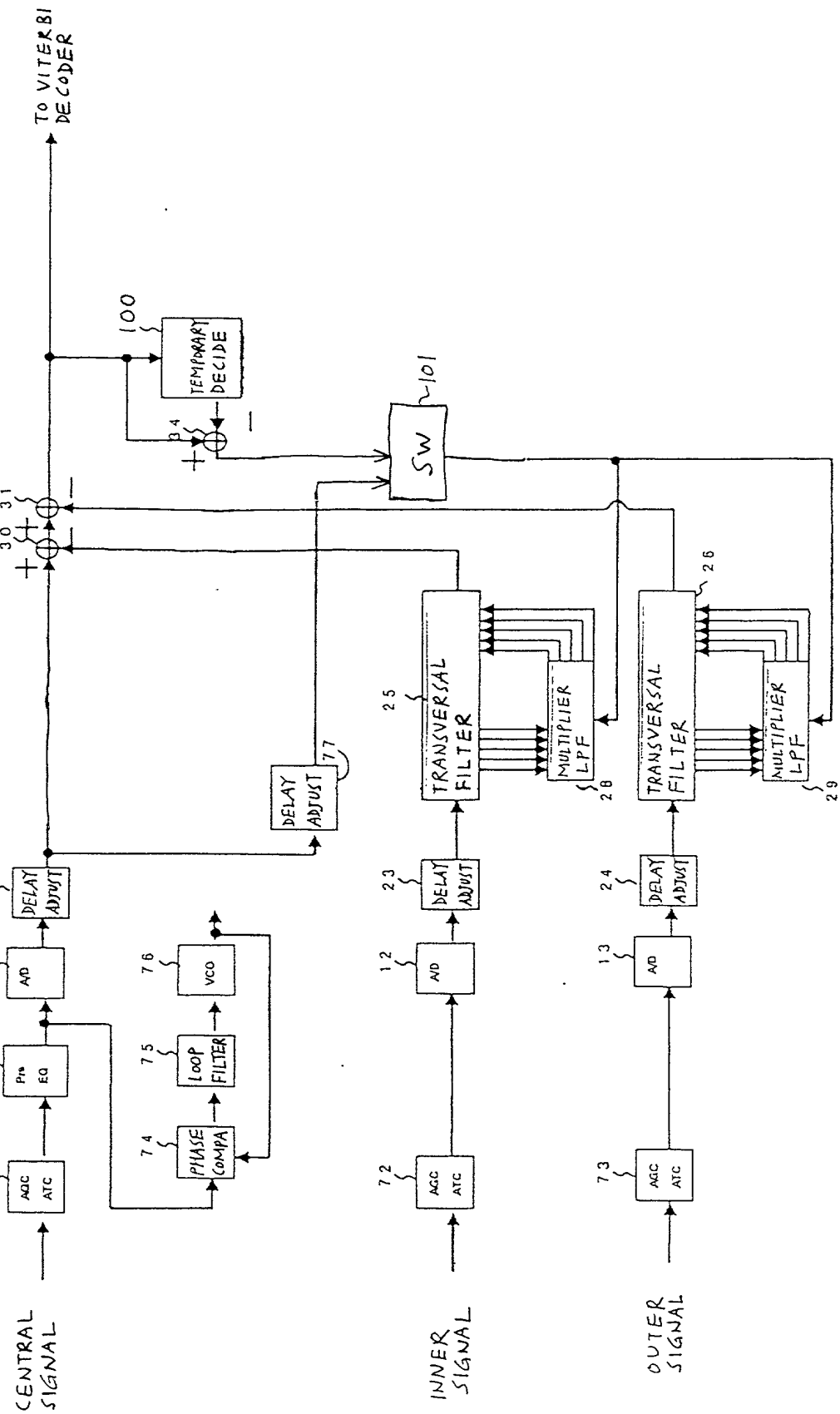

TO VITERBI DECODER
100
TEMPORARY DECIDE
34
SW
101
30
31
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
71
AGC ATC
72
AGC ATC
73
AGC ATC
41
Pre EQ
11
A/D
12
A/D
13
A/D
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
74
PHASE COMPA
75
LOOP FILTER
76
VCO
77
DELAY ADJUST
25
TRANSVERSAL FILTER
26
TRANSVERSAL FILTER
28
MULTIPLIER LPF
29
MULTIPLIER LPF

FIG. 31

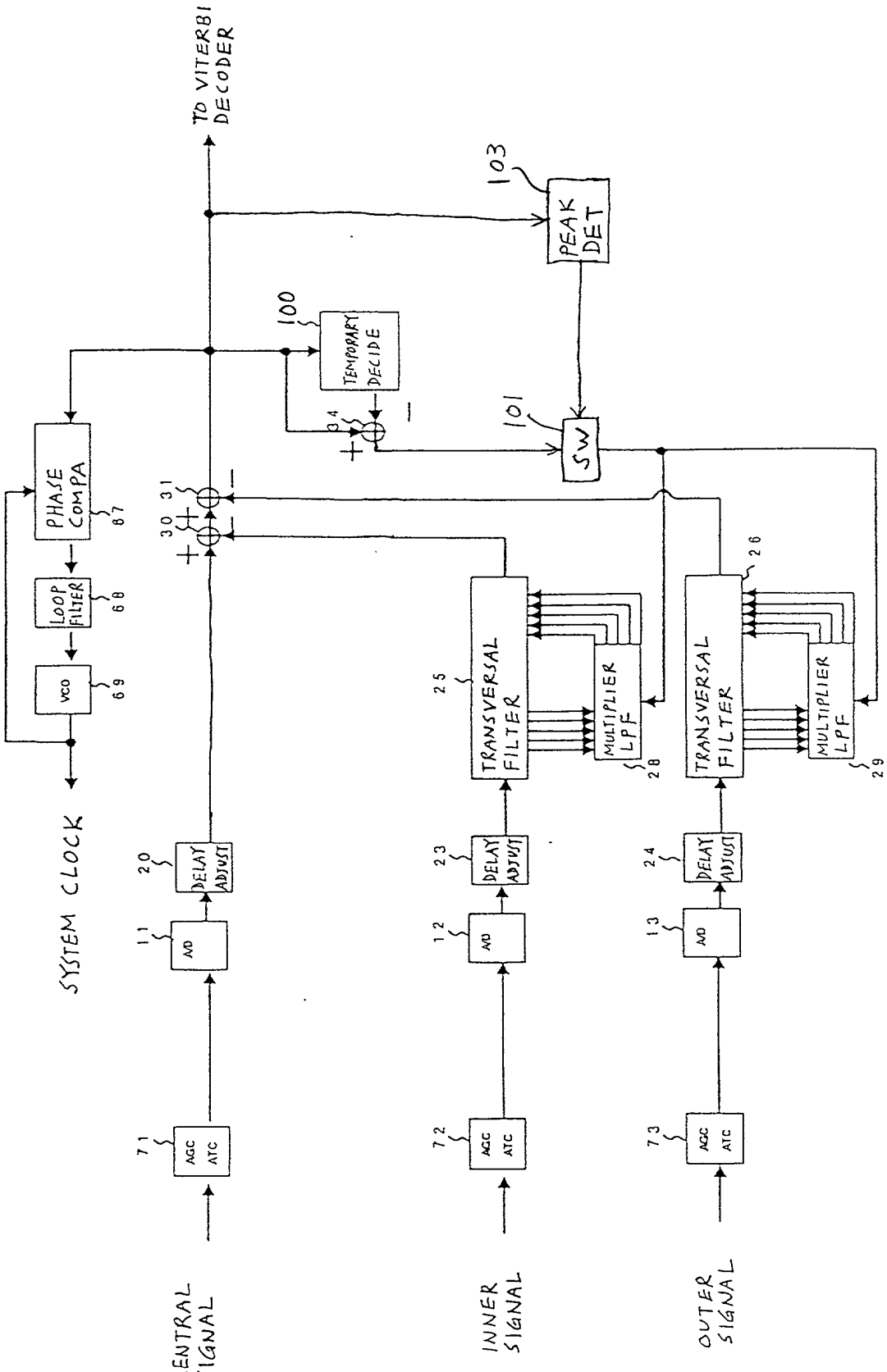
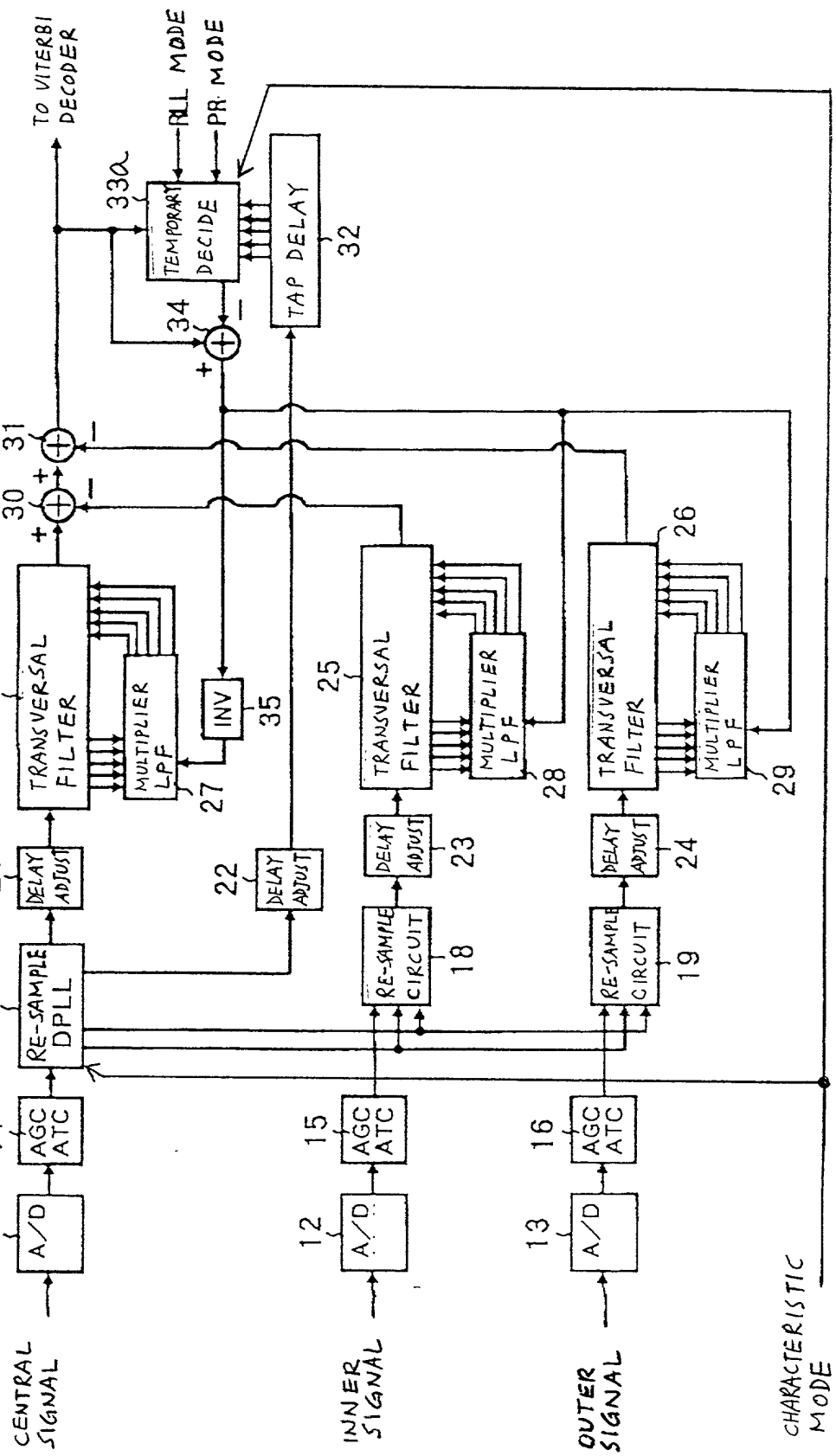

TO VITERBI DECODER
103
PEAK DET
100
TEMPORARY DECIDE
101
SW
34
30
31
PHASE COMPA
87
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
71
AGC ATC
72
AGC ATC
73
AGC ATC
11
A/D
12
A/D
13
A/D
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
25
TRANSVERSAL FILTER
26
TRANSVERSAL FILTER
28
MULTIPLIER LPF
29
MULTIPLIER LPF
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 32


TO VITERBI DECODER
RLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
AGC ATC
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

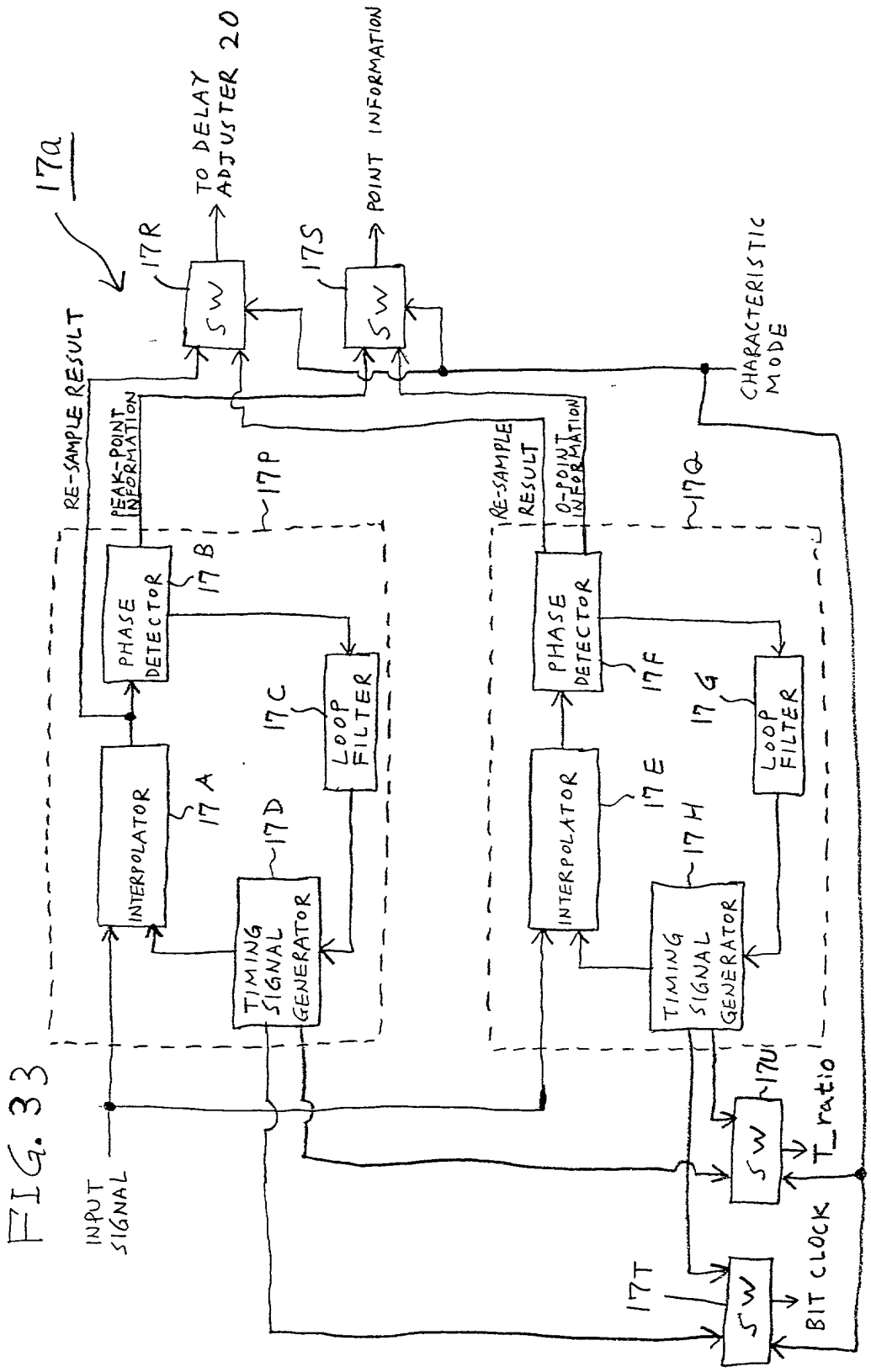

17a
TO DELAY ADJUSTER 20
POINT INFORMATION
17R
17S
SW
SW
CHARACTERISTIC MODE
RE-SAMPLE RESULT
PEAK-POINT INFORMATION
17P
RE-SAMPLE RESULT
0-POINT INFORMATION
17Q
PHASE DETECTOR
17B
PHASE DETECTOR
17F
LOOP FILTER
17C
LOOP FILTER
17G
INTERPOLATOR
17A
INTERPOLATOR
17E
TIMING SIGNAL GENERATOR
17D
TIMING SIGNAL GENERATOR
17H
INPUT SIGNAL
SW
17U
T_ratio
17T
SW
BIT CLOCK

FIG. 33

FIG. 34

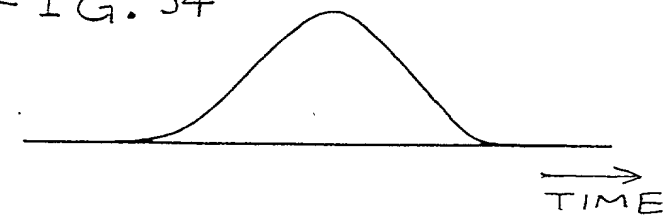


FIG. 35

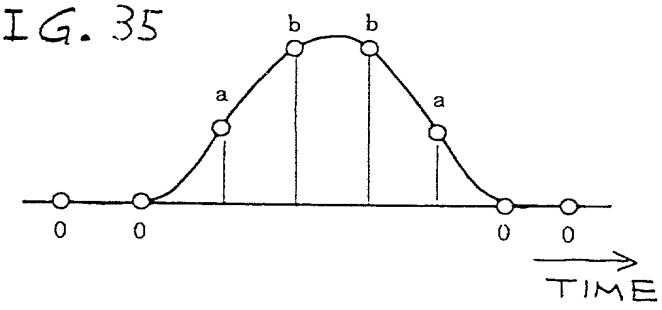


FIG. 36

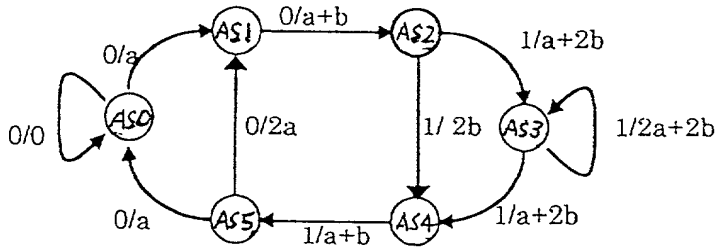


FIG. 37

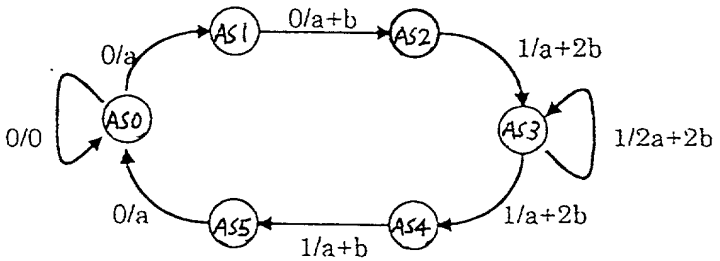


FIG. 38

RLL MODE \ PR MODE		1	2	3	4	5	6
RLL(1, X) {M1-7, MMVF, MD2}		PR(1, 1)	PR(1, 1, 1, 1)	PR(1, 2, 2, 1)	PR(1, 3, 3, 1)	PR(2, 3, 3, 2)	PR(3, 4, 4, 3)
	2a + 2b			6→+3	8→+4	10→+5	14→+7
	a + 2b			5→+2	7→+3	8→+3	11→+4
	2b			4→+1	6→+2	6→+1	8→+1
	a + b			3→0	4→0	5→0	7→0
	2a			2→−1	2→−2	4→−1	6→−1
	a			1→−2	1→−3	2→−3	3→−4
	0			0→−3	0→−4	0→−5	0→−7
	GAIN G	A	A/2	A/3	A/4	A/5	A/7
RLL(2, X) {EFM, EFMP, M8-15, PR}	2a + 2b		4→+2	6→+3	8→+4	10→+5	14→+7
	a + 2b	2→+1	3→+1	5→+2	7→+3	8→+3	11→+4
	a + b	1→0	2→0	3→0	4→0	5→0	7→0
	a	0→−1	1→−1	1→−2	1→−3	2→−3	3→−4
	0		0→−2	0→−3	0→−4	0→−5	0→−7

FIG. 39

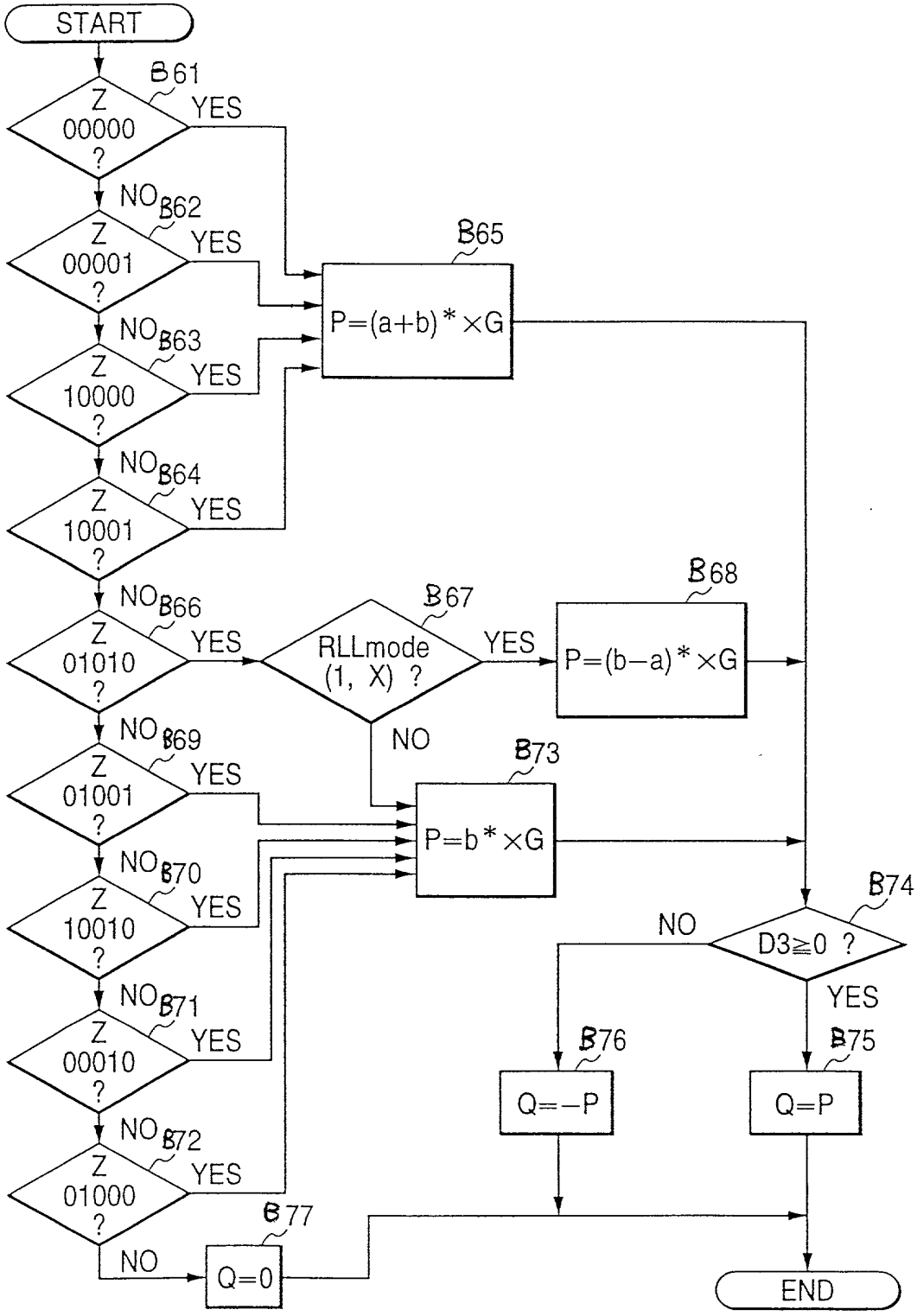

START
B61
Z 00000 ?
YES
NO
B62
Z 00001 ?
YES
NO
B63
Z 10000 ?
YES
NO
B64
Z 10001 ?
YES
NO
B65
P=(a+b)*×G
B66
Z 01010 ?
YES
NO
B67
RLLmode (1, X) ?
YES
NO
B68
P=(b−a)*×G
B69
Z 01001 ?
YES
NO
B70
Z 10010 ?
YES
NO
B71
Z 00010 ?
YES
NO
B72
Z 01000 ?
YES
NO
B73
P=b*×G
B74
D3≧0 ?
YES
NO
B75
Q=P
B76
Q=−P
B77
Q=0
END

FIG. 40

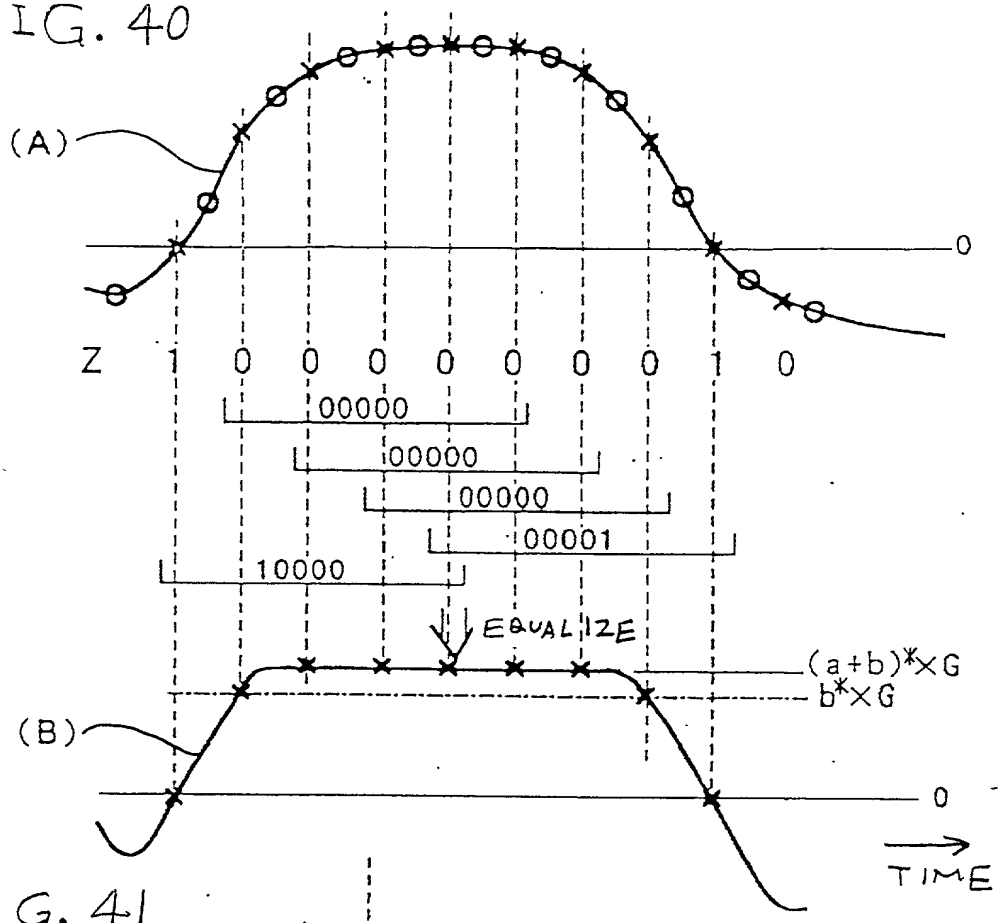

(A)
0
Z 1 0 0 0 0 0 0 0 1 0
00000
00000
00000
00001
10000
EQUALIZE
(a+b)*×G
b*×G
(B)
0
TIME

FIG. 41

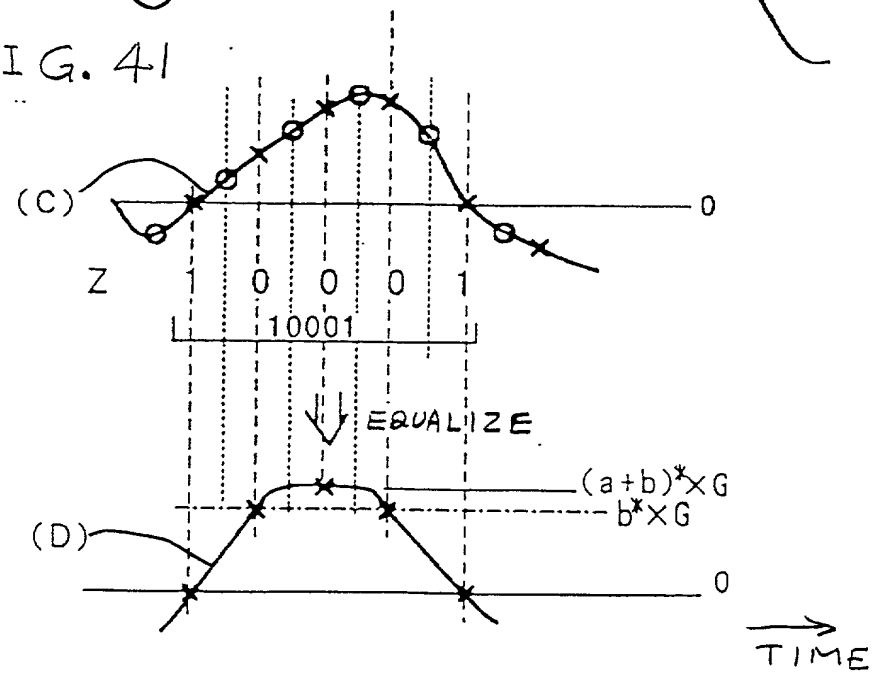

(C)
0
Z 1 0 0 0 1
10001
EQUALIZE
(a+b)*×G
b*×G
(D)
0
TIME

FIG. 42

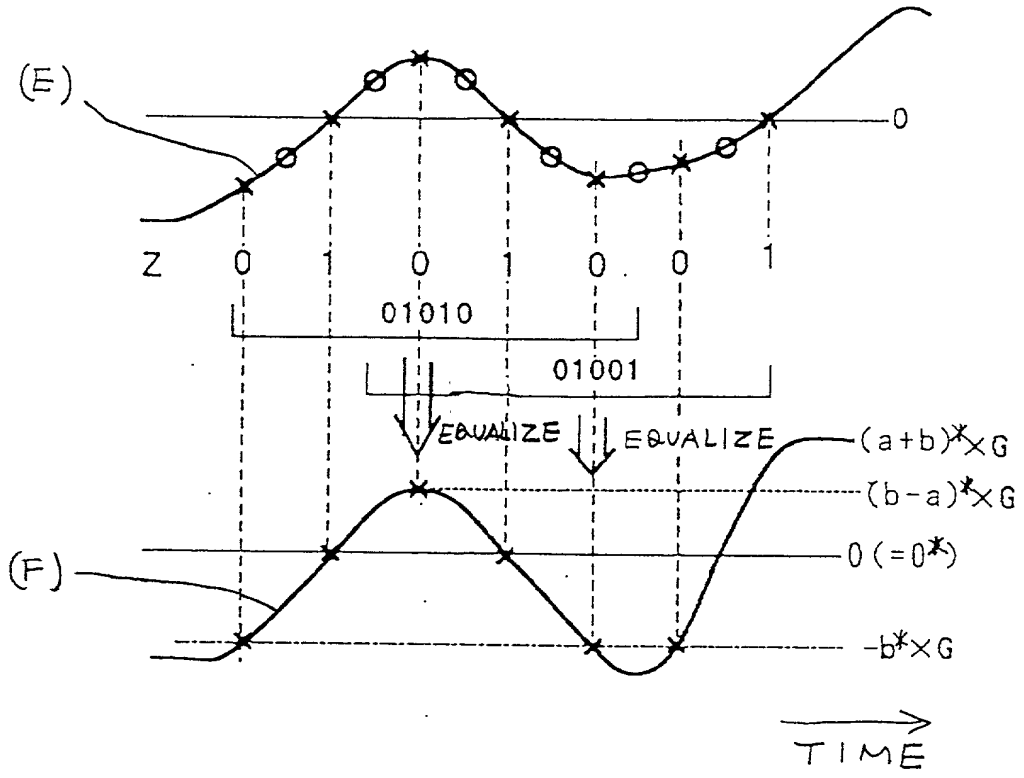

(E)
0
Z
0
1
0
1
0
0
1
01010
01001
EQUALIZE
EQUALIZE
(a+b)*×G
(b-a)*×G
0 (=0*)
(F)
-b*×G
TIME

FIG. 43

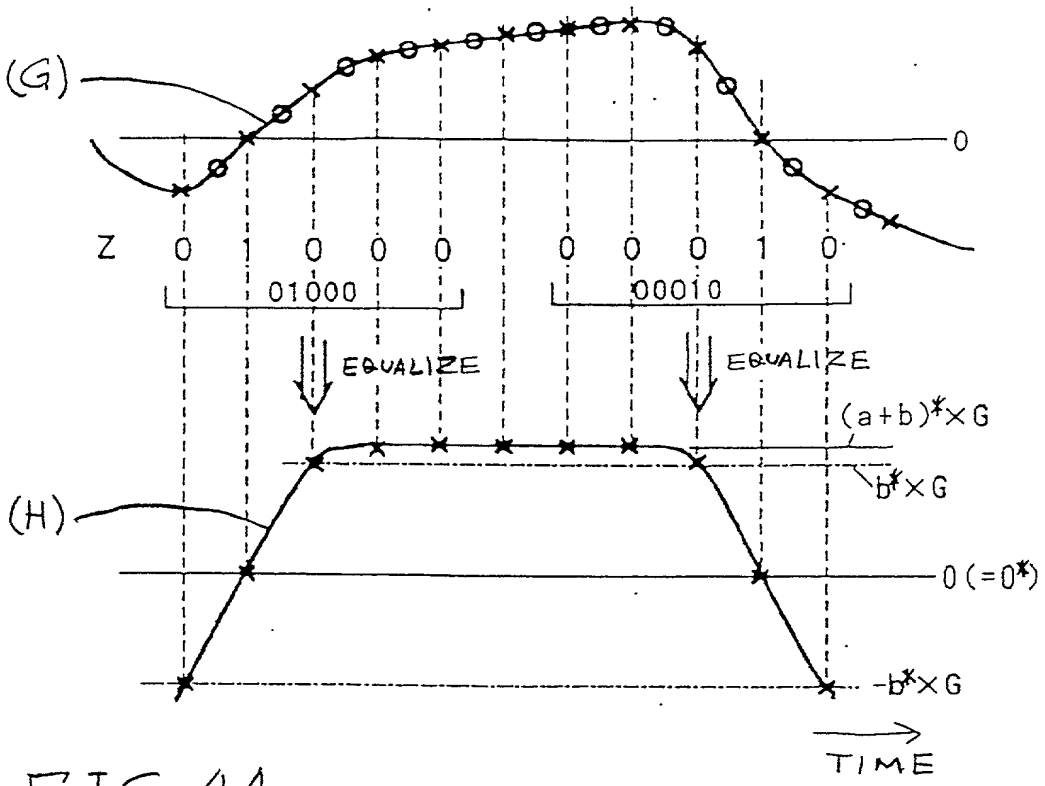

(G)
0
Z 0 1 0 0 0 0 0 0 1 0
01000
00010
EQUALIZE
EQUALIZE
(a+b)*×G
b*×G
(H)
0 (=0*)
-b*×G
TIME

FIG. 44

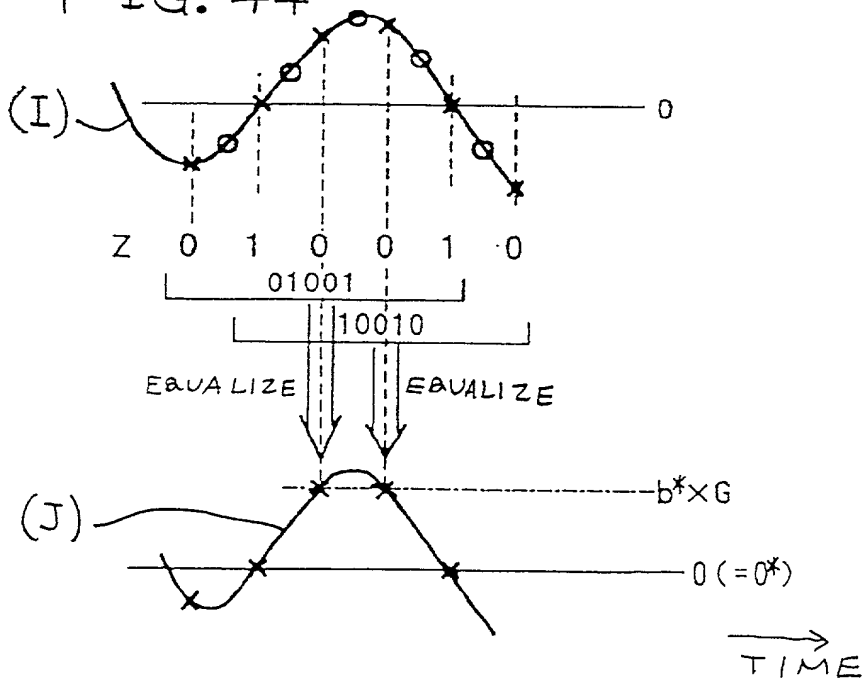

(I)
0
Z 0 1 0 0 1 0
01001
10010
EQUALIZE
EQUALIZE
b*×G
(J)
0 (=0*)
TIME

FIG. 45

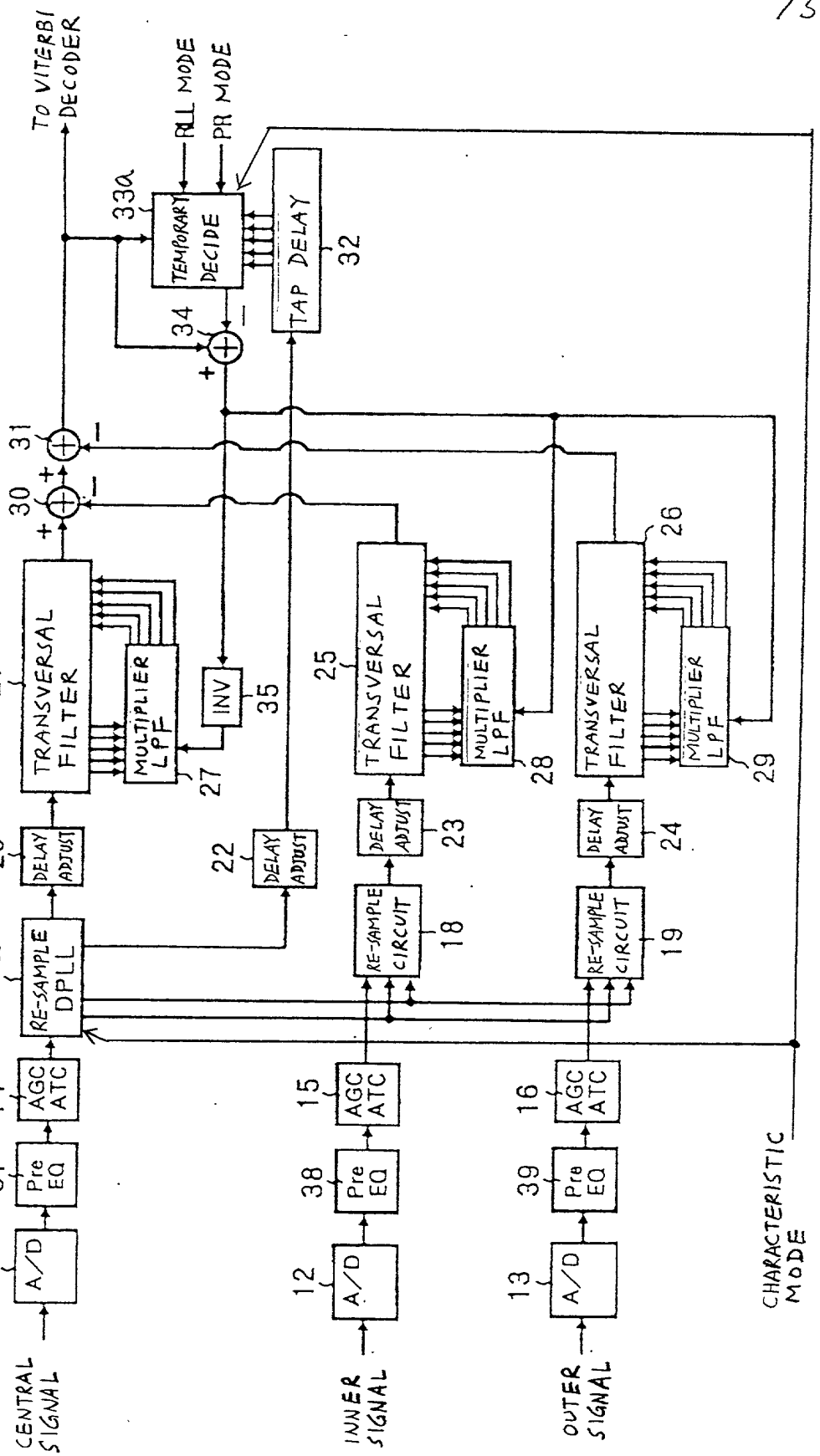

TO VITERBI DECODER
ALL MODE
PR MODE
33a
TEMPORARY DECIDE
34
TAP DELAY
32
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
22
DELAY ADJUST
DELAY ADJUST
23
DELAY ADJUST
24
17a
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
18
RE-SAMPLE CIRCUIT
19
14
AGC ATC
15
AGC ATC
16
AGC ATC
37
Pre EQ
38
Pre EQ
39
Pre EQ
11
A/D
12
A/D
13
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 46

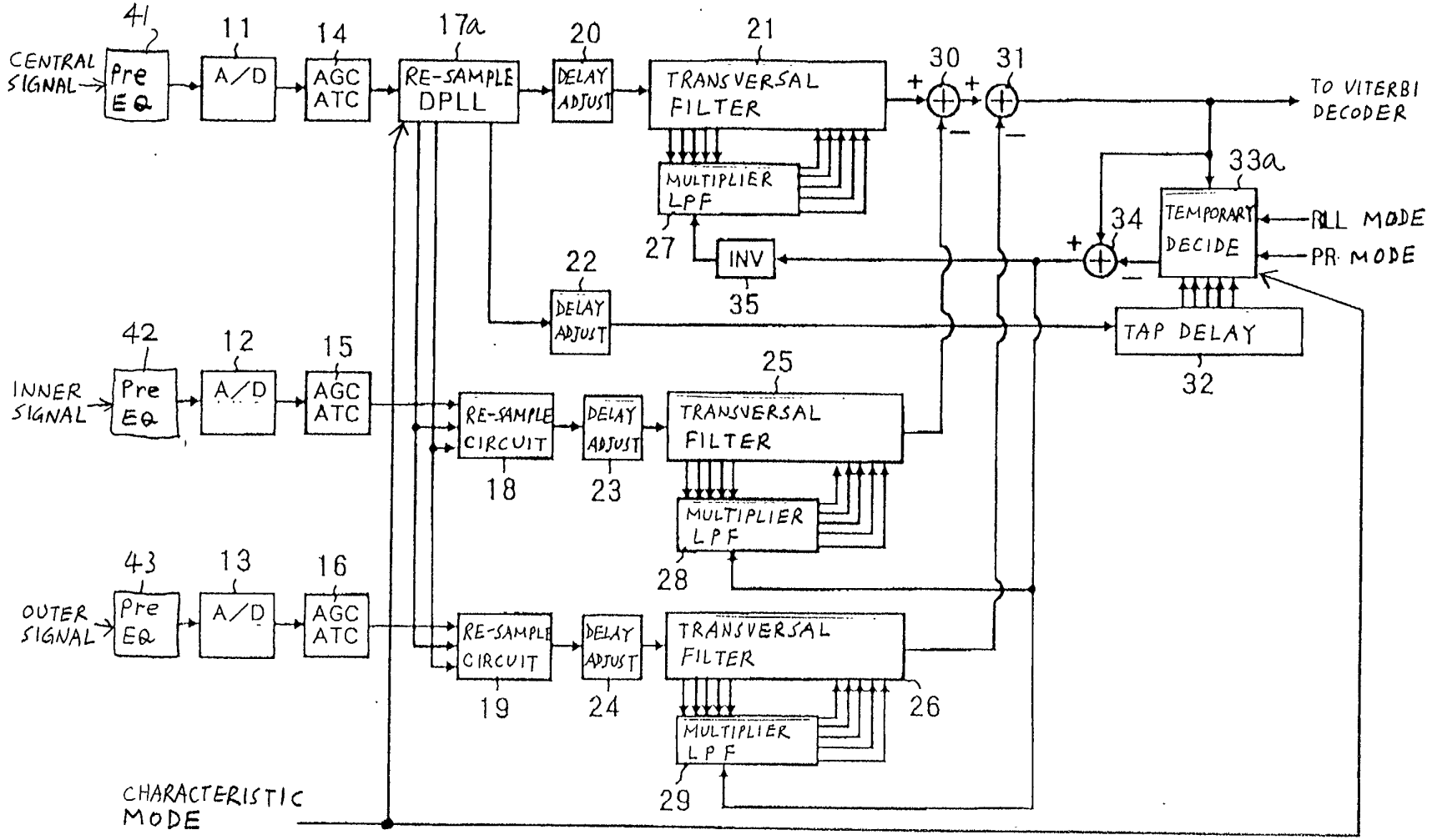

41
CENTRAL SIGNAL
Pre EQ
11
A/D
14
AGC ATC
17a
RE-SAMPLE DPLL
20
DELAY ADJUST
21
TRANSVERSAL FILTER
30
31
TO VITERBI DECODER
MULTIPLIER LPF
27
INV
35
22
DELAY ADJUST
33a
TEMPORARY DECIDE
34
PLL MODE
PR MODE
TAP DELAY
32
42
INNER SIGNAL
Pre EQ
12
A/D
15
AGC ATC
RE-SAMPLE CIRCUIT
18
DELAY ADJUST
23
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
43
OUTER SIGNAL
Pre EQ
13
A/D
16
AGC ATC
RE-SAMPLE CIRCUIT
19
DELAY ADJUST
24
TRANSVERSAL FILTER
26
MULTIPLIER LPF
29
CHARACTERISTIC MODE

FIG. 47

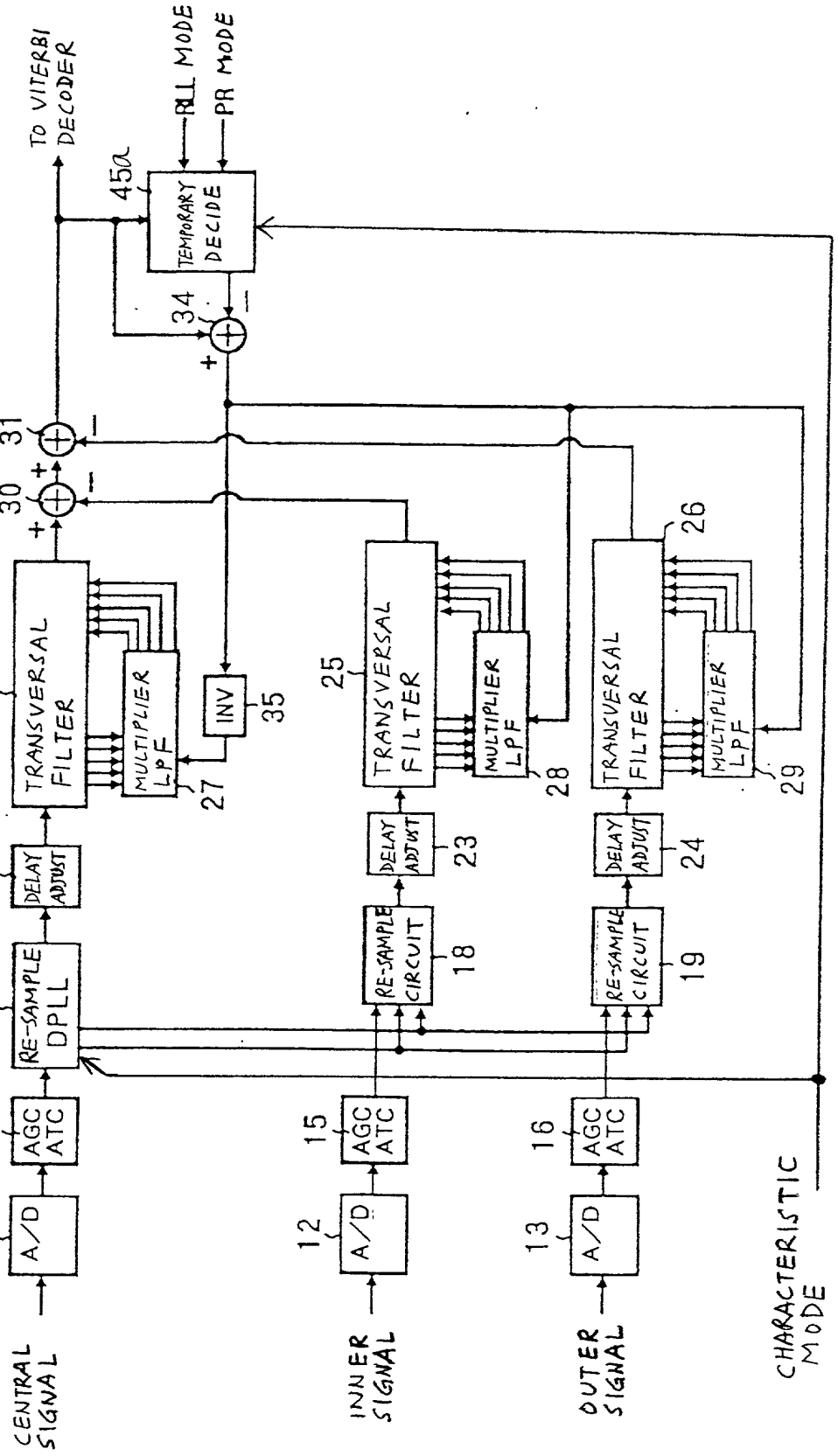

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE
A/D
AGC ATC
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
TO VITERBI DECODER
PR MODE
RLL MODE
11
12
13
14
15
16
17a
18
19
20
21
23
24
25
26
27
28
29
30
31
34
35
45a

FIG. 48

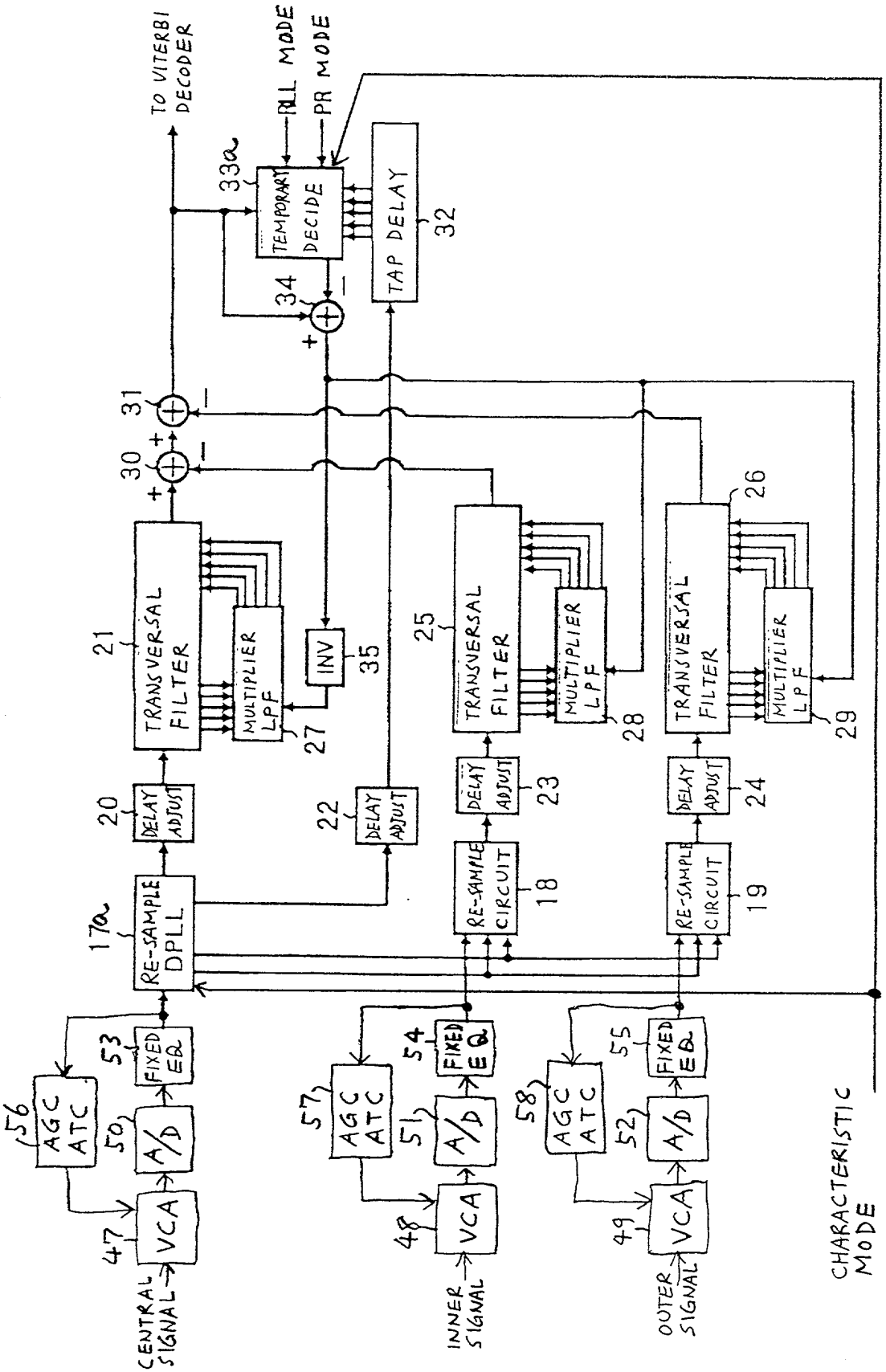

TO VITERBI DECODER
PLL MODE
PR MODE
33a
TEMPORARY DECIDE
34
TAP DELAY
32
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
22
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
17a
RE-SAMPLE DPLL
18
RE-SAMPLE CIRCUIT
19
RE-SAMPLE CIRCUIT
53
FIXED EQ
54
FIXED EQ
55
FIXED EQ
56
AGC ATC
50
A/D
47
VCA
CENTRAL SIGNAL
57
AGC ATC
51
A/D
48
VCA
INNER SIGNAL
58
AGC ATC
52
A/D
49
VCA
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 49

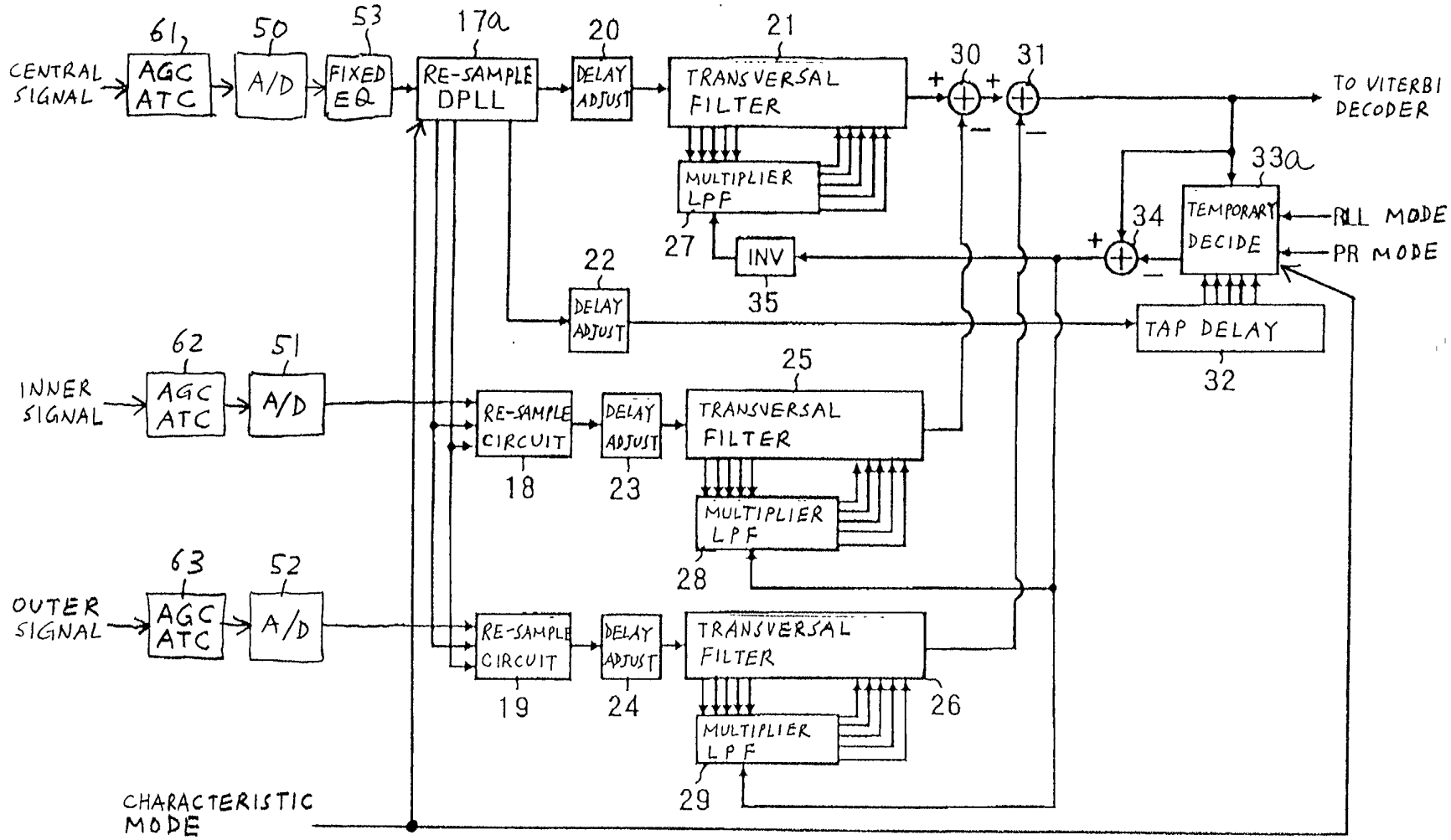

CENTRAL SIGNAL
AGC ATC
61
A/D
50
FIXED EQ
53
RE-SAMPLE DPLL
17a
DELAY ADJUST
20
TRANSVERSAL FILTER
21
30
31
TO VITERBI DECODER
MULTIPLIER LPF
27
INV
35
33a
TEMPORARY DECIDE
34
PLL MODE
PR MODE
22
DELAY ADJUST
TAP DELAY
32
INNER SIGNAL
AGC ATC
62
A/D
51
RE-SAMPLE CIRCUIT
18
DELAY ADJUST
23
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
OUTER SIGNAL
AGC ATC
63
A/D
52
RE-SAMPLE CIRCUIT
19
DELAY ADJUST
24
TRANSVERSAL FILTER
26
MULTIPLIER LPF
29
CHARACTERISTIC MODE

FIG. 50

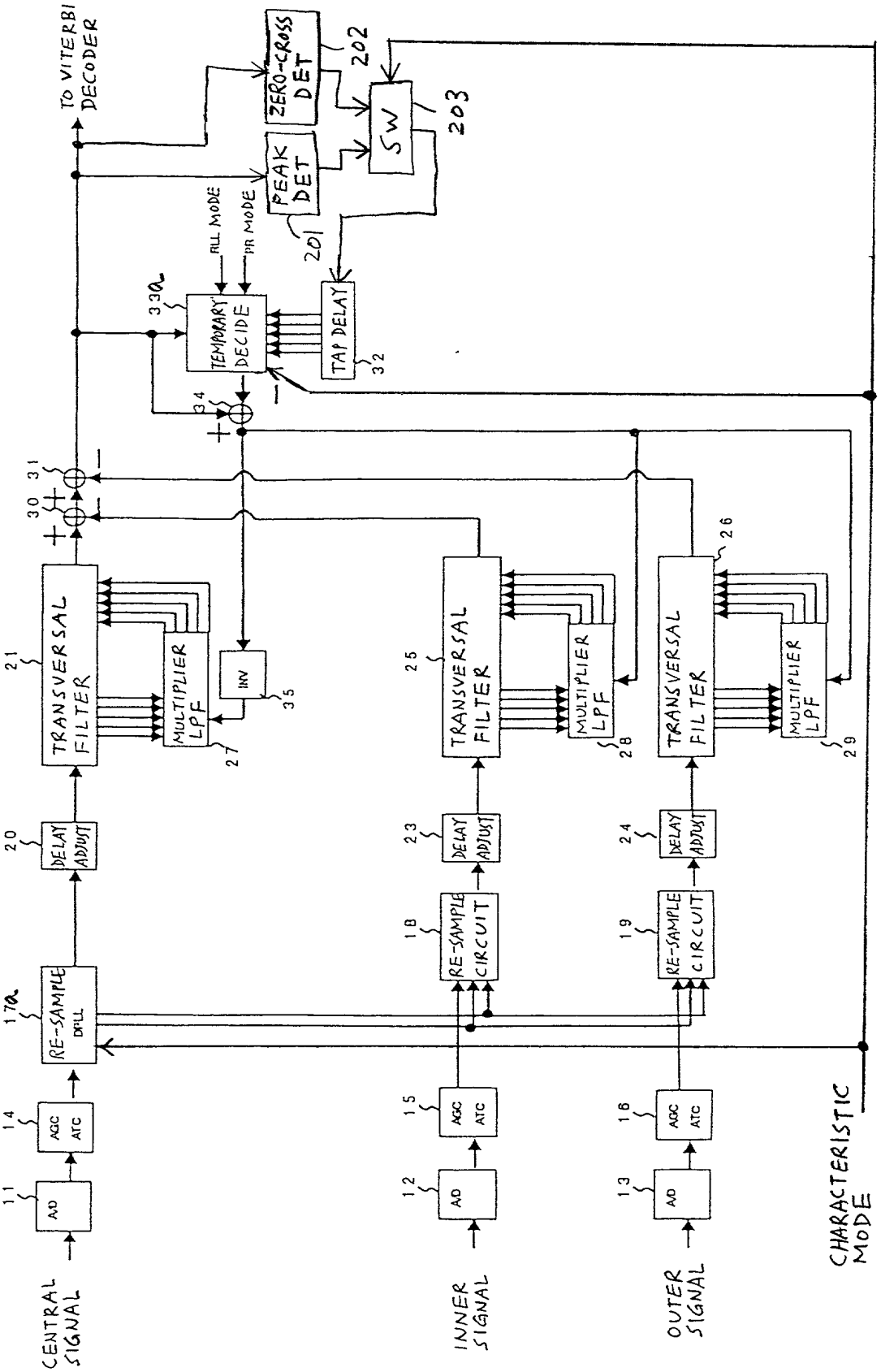

TO VITERBI DECODER
ZERO-CROSS DET
202
PEAK DET
SW
203
201
FULL MODE
PR MODE
33a
TEMPORARY DECIDE
TAP DELAY
32
34
30
31
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
17a
RE-SAMPLE FULL
18
RE-SAMPLE CIRCUIT
19
RE-SAMPLE CIRCUIT
14
AGC ATC
15
AGC ATC
16
AGC ATC
11
A/D
12
A/D
13
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 51

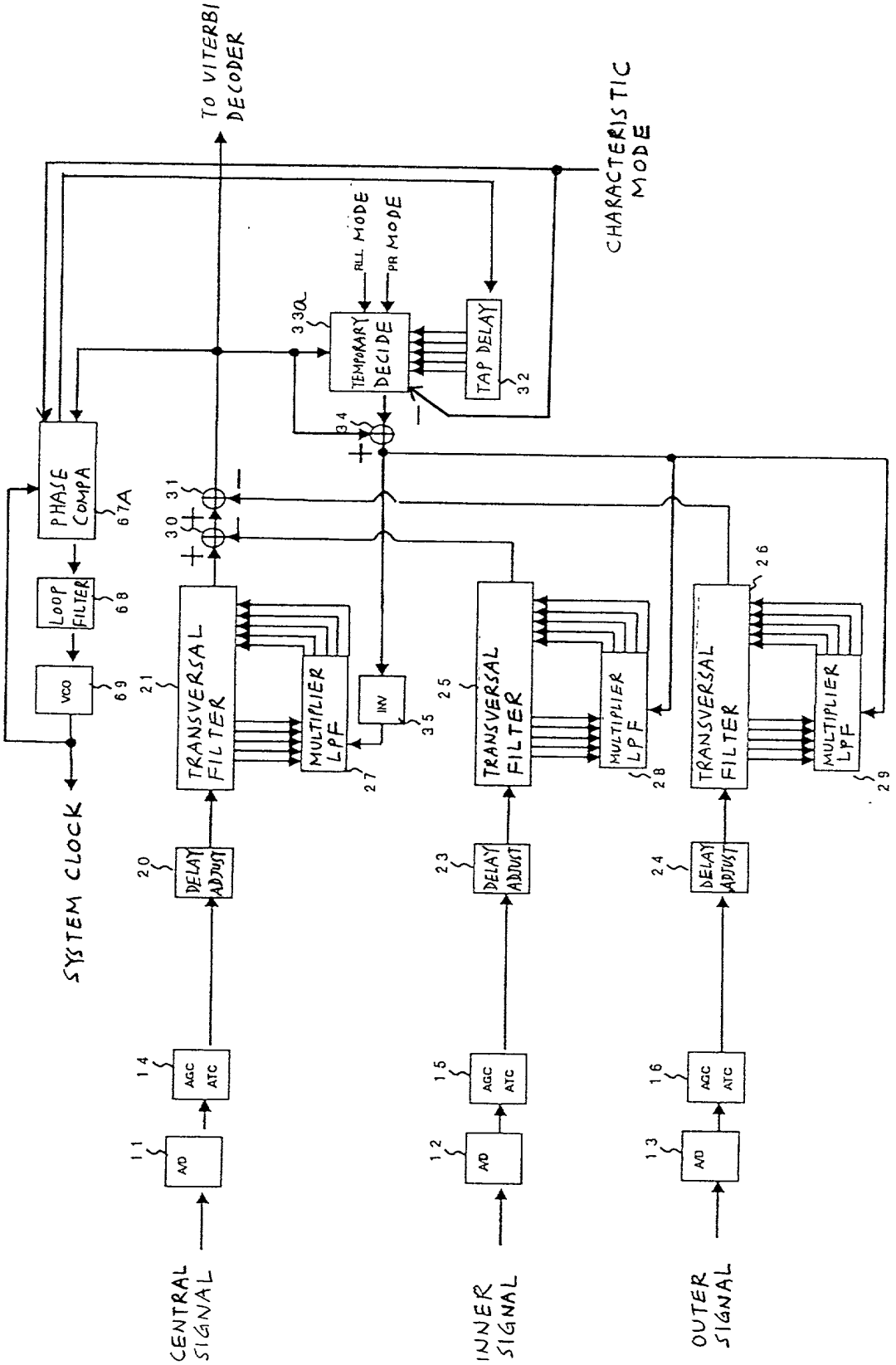

TO VITERBI DECODER
CHARACTERISTIC MODE
RLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
PHASE COMPA
LOOP FILTER
VCO
SYSTEM CLOCK
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
DELAY ADJUST
AGC ATC
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 52

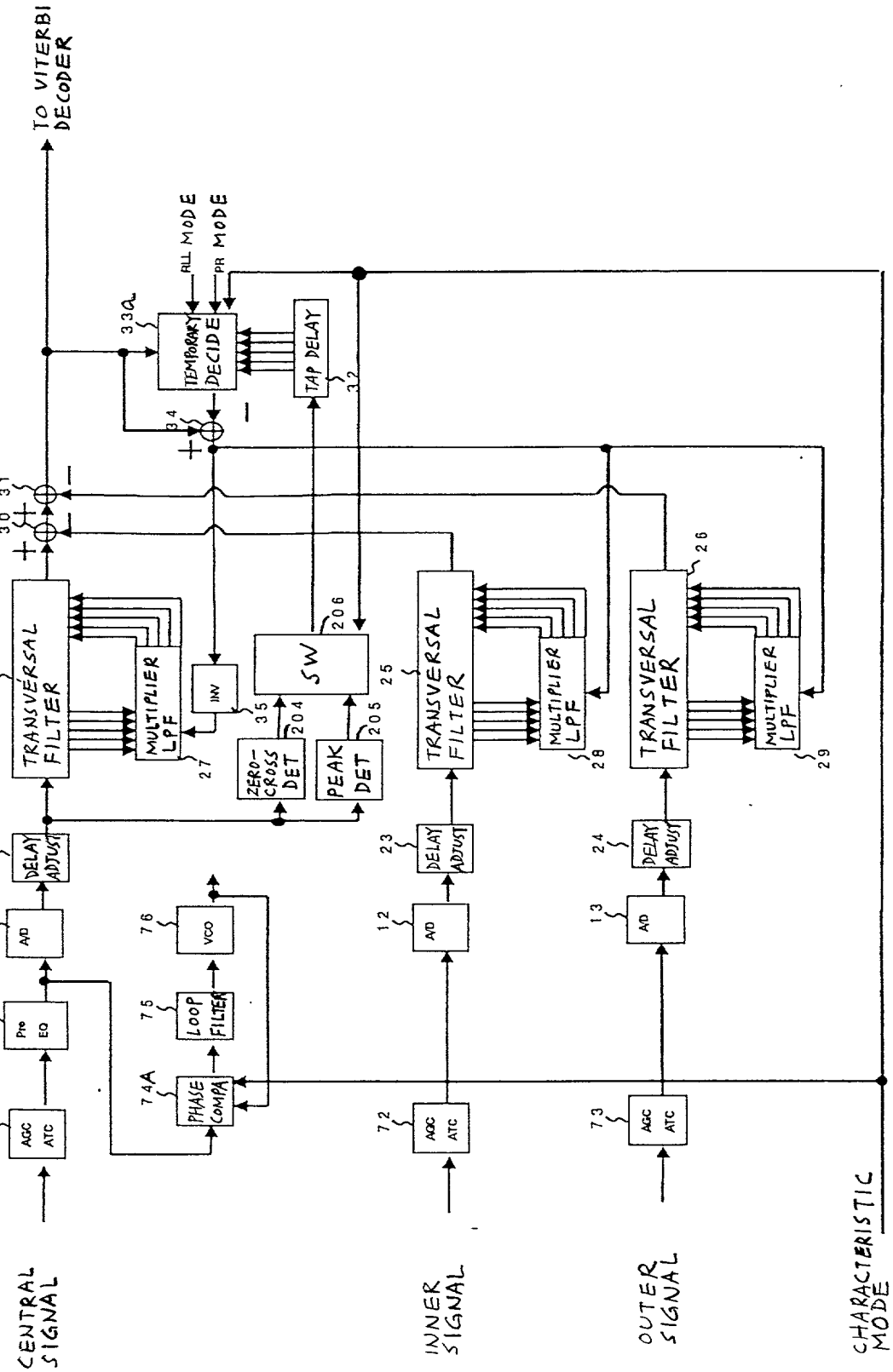

TO VITERBI DECODER
ALL MODE
PR MODE
33a
TEMPORARY DECIDE
TAP DELAY
32
34
30
31
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
SW
206
ZERO-CROSS DET
204
PEAK DET
205
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
11
A/D
41
Pre EQ
71
AGC ATC
CENTRAL SIGNAL
76
VCO
75
LOOP FILTER
74A
PHASE COMPA
23
DELAY ADJUST
12
A/D
72
AGC ATC
INNER SIGNAL
24
DELAY ADJUST
13
A/D
73
AGC ATC
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 53

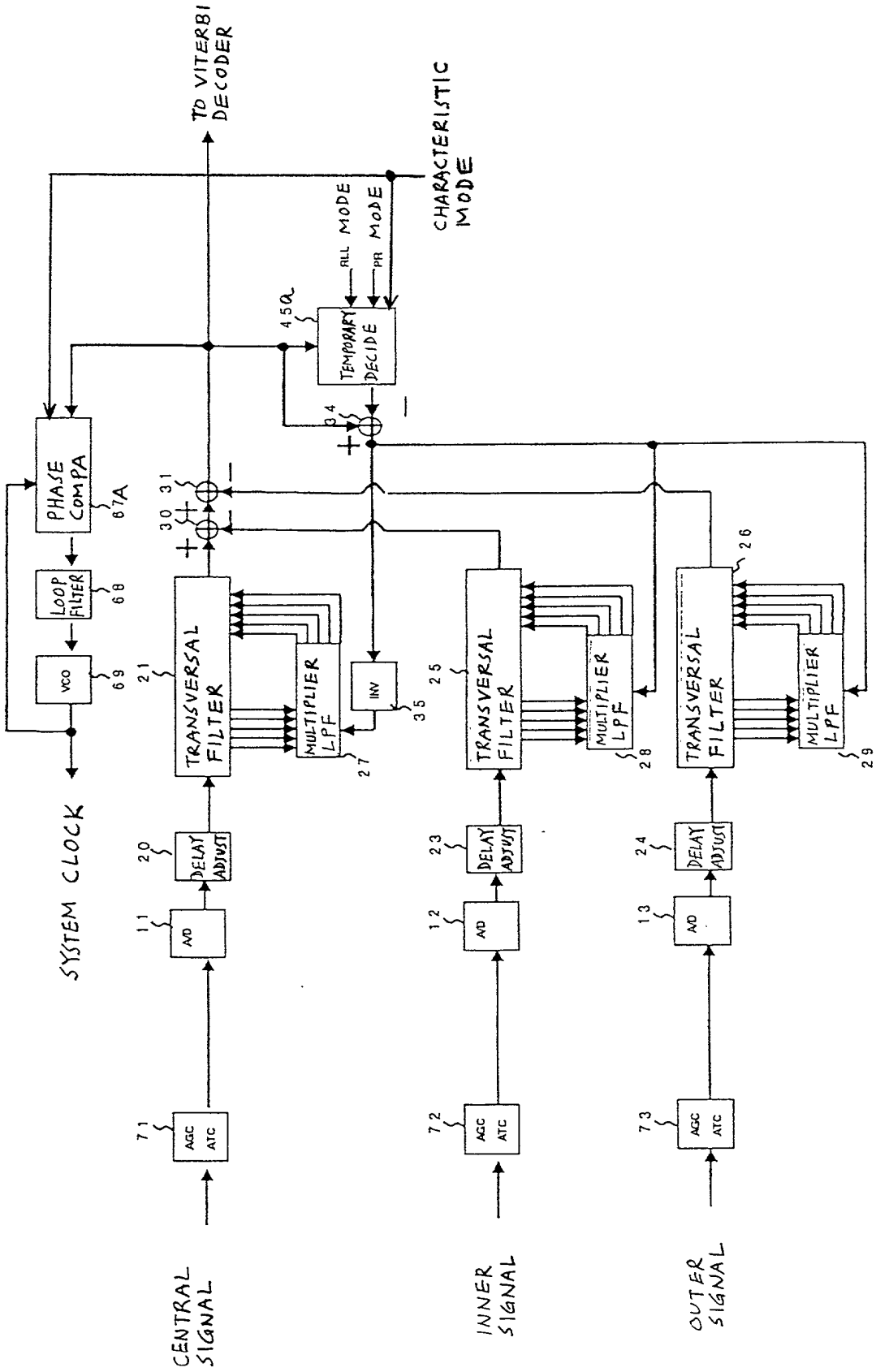

TO VITERBI DECODER
CHARACTERISTIC MODE
ALL MODE
PR MODE
TEMPORARY DECIDE
45a
34
PHASE COMPA
67A
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
30
31
TRANSVERSAL FILTER
21
MULTIPLIER LPF
27
INV
35
25
28
26
29
DELAY ADJUST
20
23
24
A/D
11
12
13
AGC ATC
71
72
73
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 54

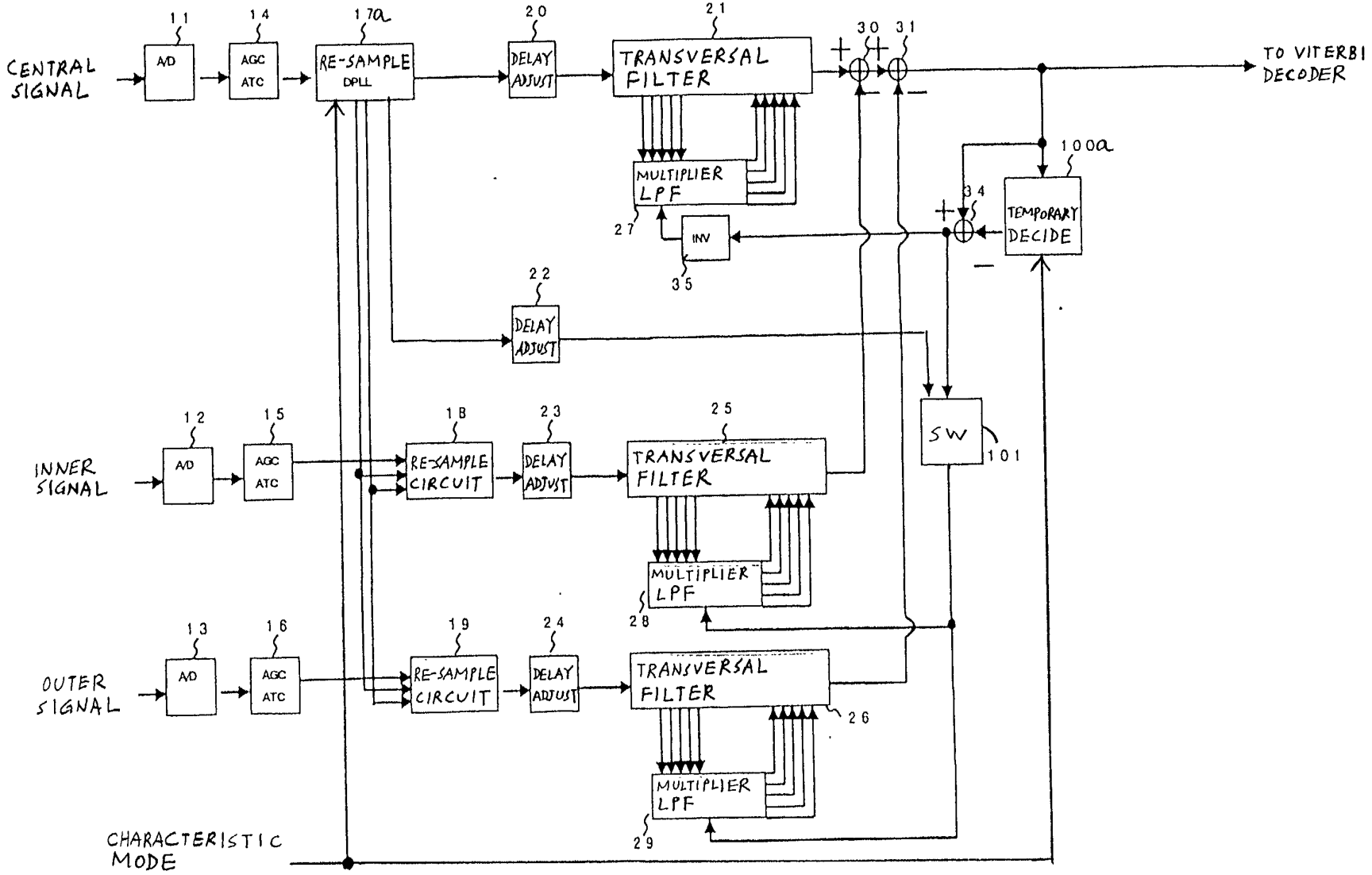

CENTRAL SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
DELAY ADJUST
TRANSVERSAL FILTER
TO VITERBI DECODER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
DELAY ADJUST
INNER SIGNAL
A/D
AGC ATC
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
SW
MULTIPLIER LPF
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
CHARACTERISTIC MODE
11
14
17a
20
21
30
31
100a
34
27
35
22
12
15
18
23
25
101
28
13
16
19
24
26
29

FIG. 55

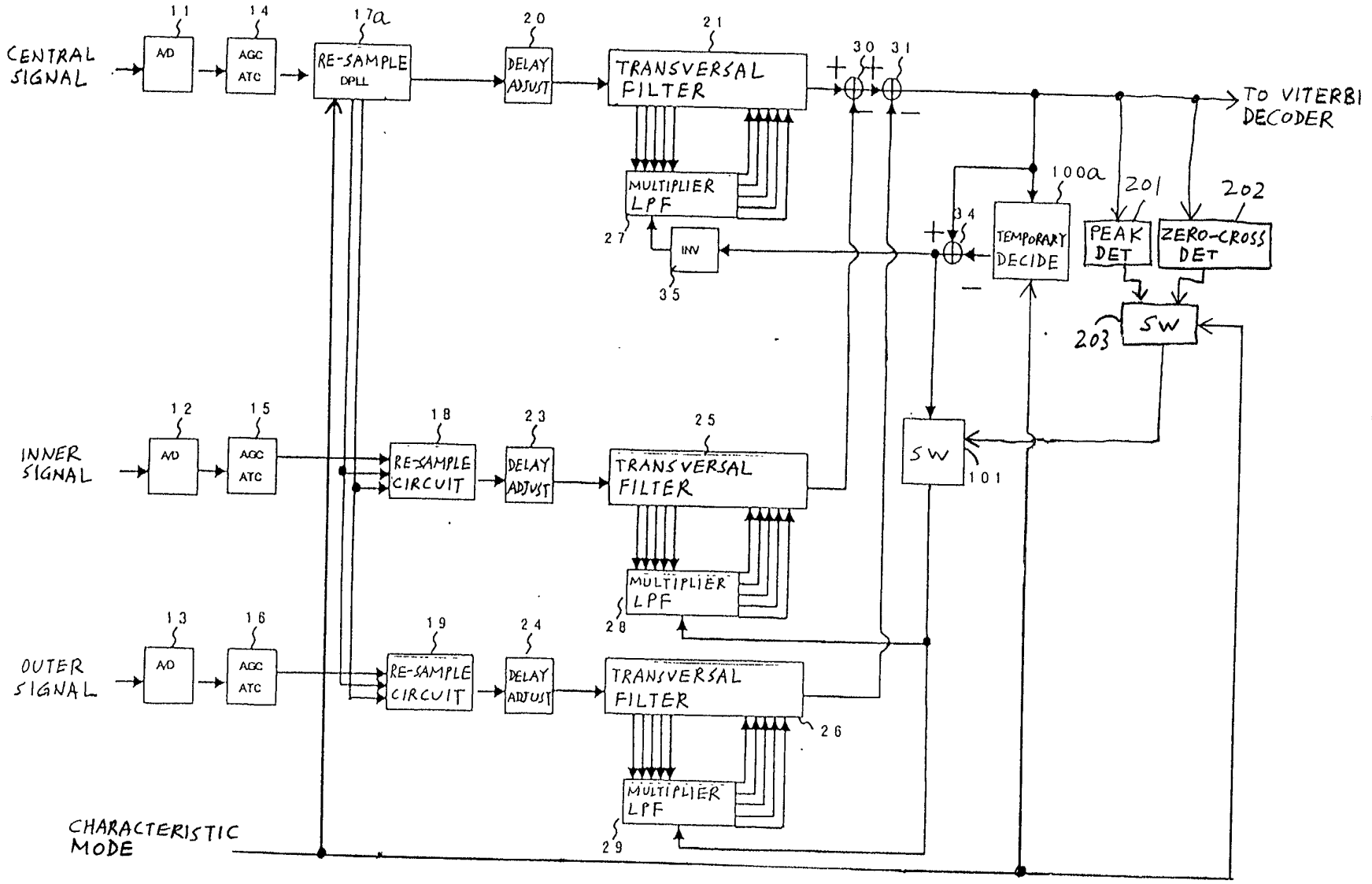

CENTRAL SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
PEAK DET
ZERO-CROSS DET
SW
TO VITERBI DECODER
INNER SIGNAL
RE-SAMPLE CIRCUIT
OUTER SIGNAL
CHARACTERISTIC MODE
11
12
13
14
15
16
17a
18
19
20
21
23
24
25
26
27
28
29
30
31
34
35
100a
101
201
202
203

FIG. 56

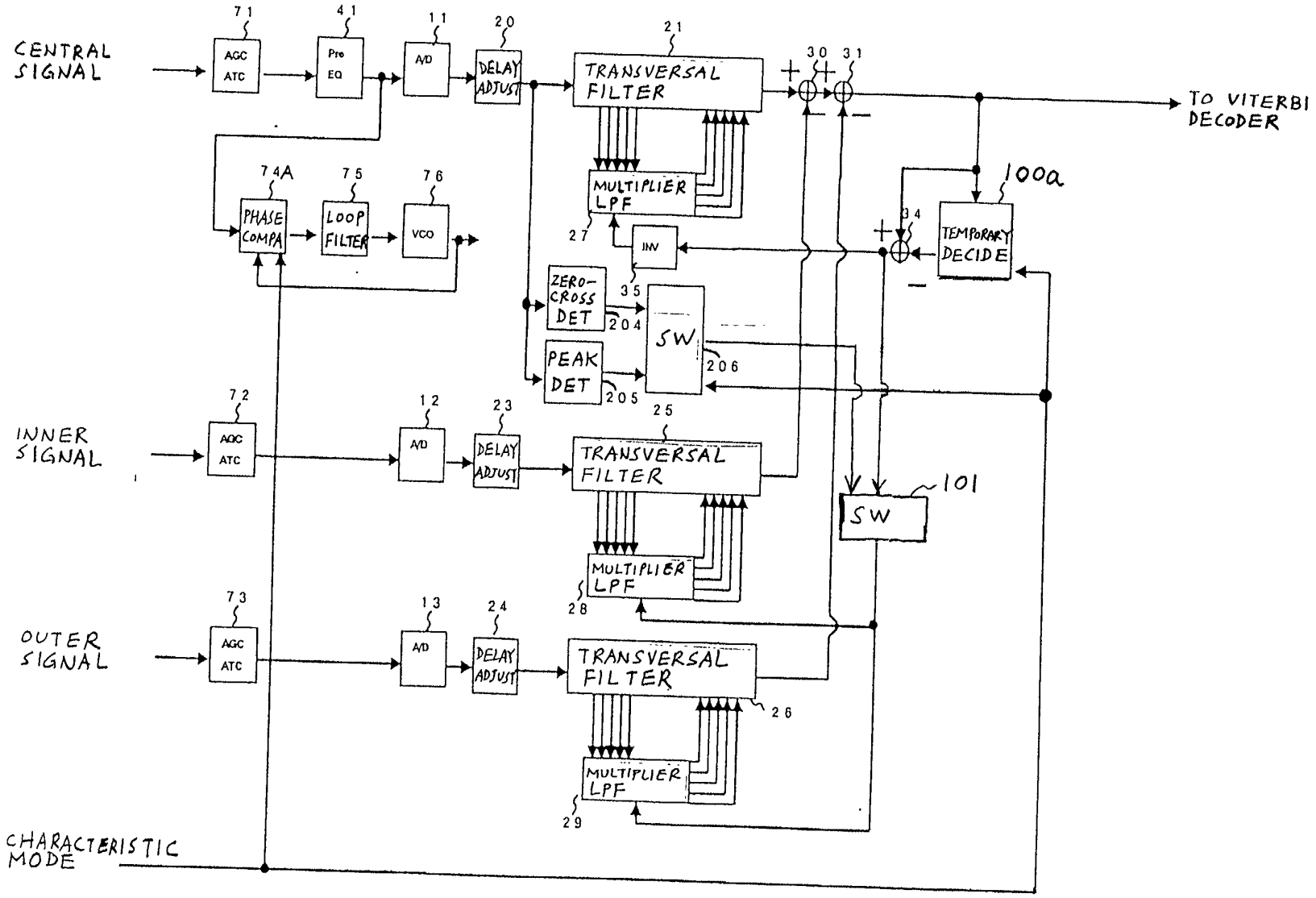

CENTRAL SIGNAL
AGC ATC
Pre EQ
A/D
DELAY ADJUST
TRANSVERSAL FILTER
TO VITERBI DECODER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
100a
PHASE COMPA
LOOP FILTER
VCO
ZERO-CROSS DET
PEAK DET
SW
INNER SIGNAL
OUTER SIGNAL
101
CHARACTERISTIC MODE

FIG. 57

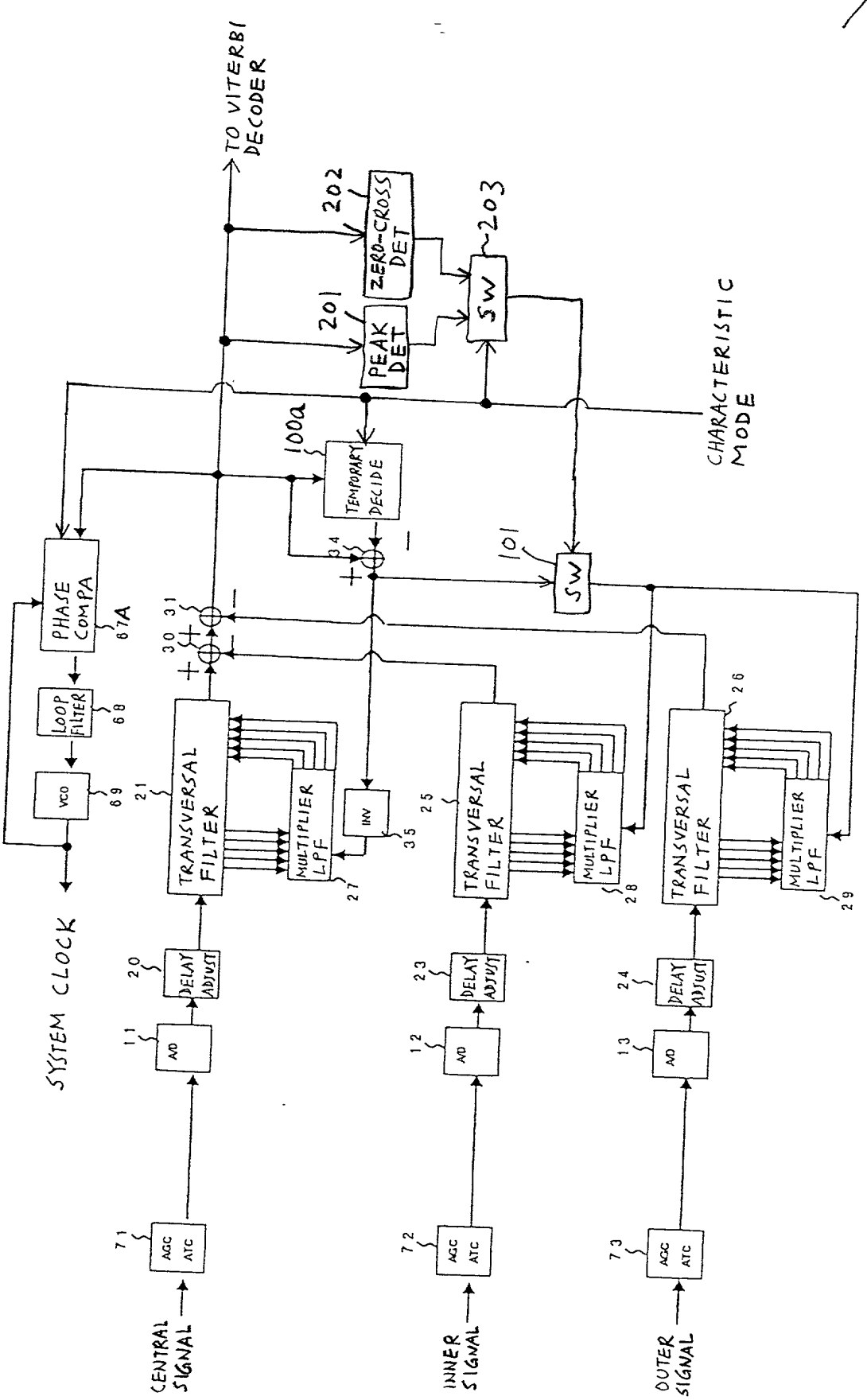

TO VITERBI DECODER
202
ZERO-CROSS DET
203
SW
201
PEAK DET
CHARACTERISTIC MODE
100a
TEMPORARY DECIDE
34
101
SW
PHASE COMPA
67A
30
31
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
11
A/D
71
AGC ATC
CENTRAL SIGNAL
23
DELAY ADJUST
12
A/D
72
AGC ATC
INNER SIGNAL
24
DELAY ADJUST
13
A/D
73
AGC ATC
OUTER SIGNAL

FIG. 58

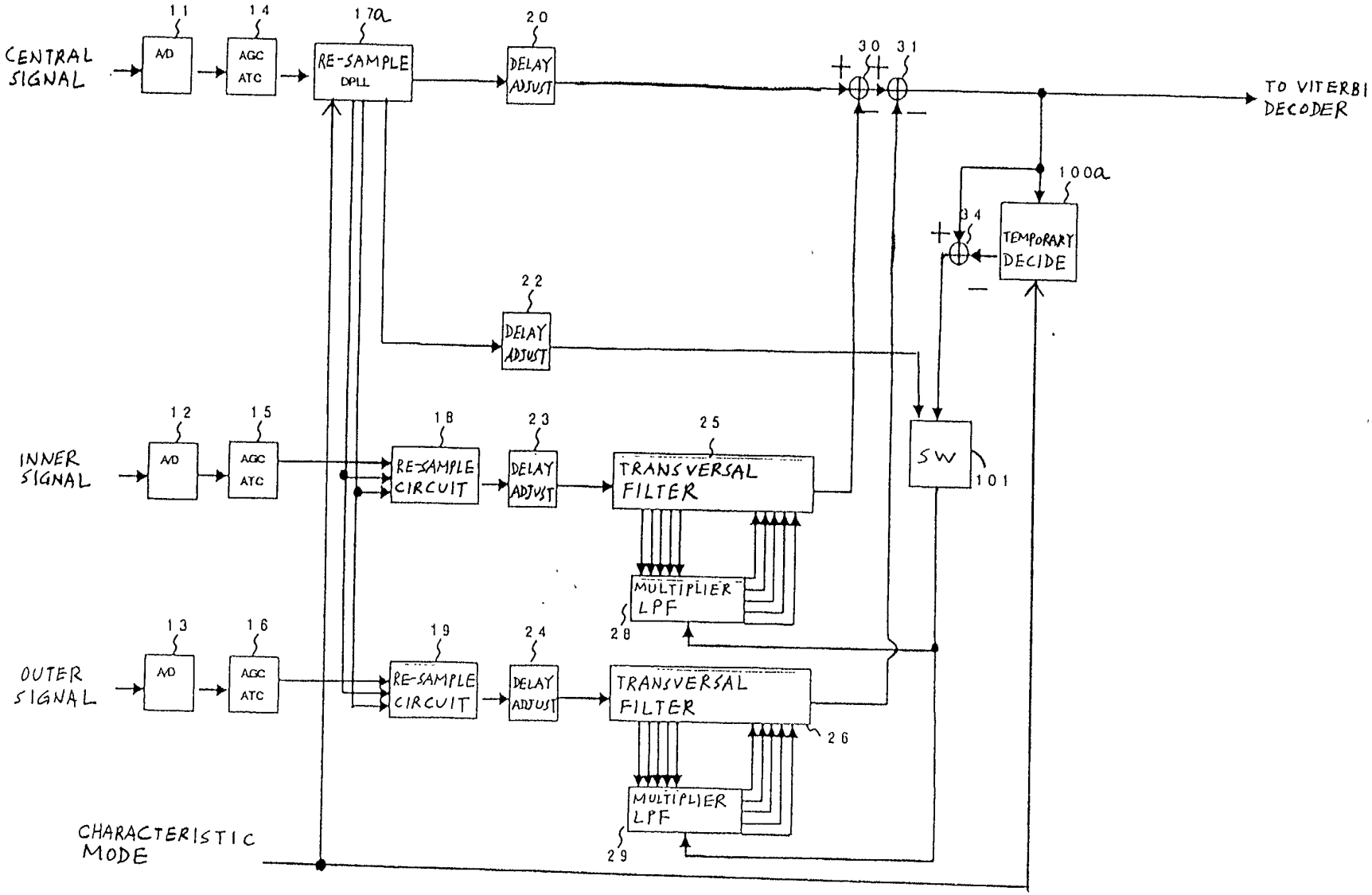

CENTRAL SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
DELAY ADJUST
TO VITERBI DECODER
TEMPORARY DECIDE
INNER SIGNAL
RE-SAMPLE CIRCUIT
TRANSVERSAL FILTER
SW
MULTIPLIER LPF
OUTER SIGNAL
CHARACTERISTIC MODE
11
14
17a
20
30
31
100a
34
22
12
15
18
23
25
101
28
13
16
19
24
26
29

FIG. 59

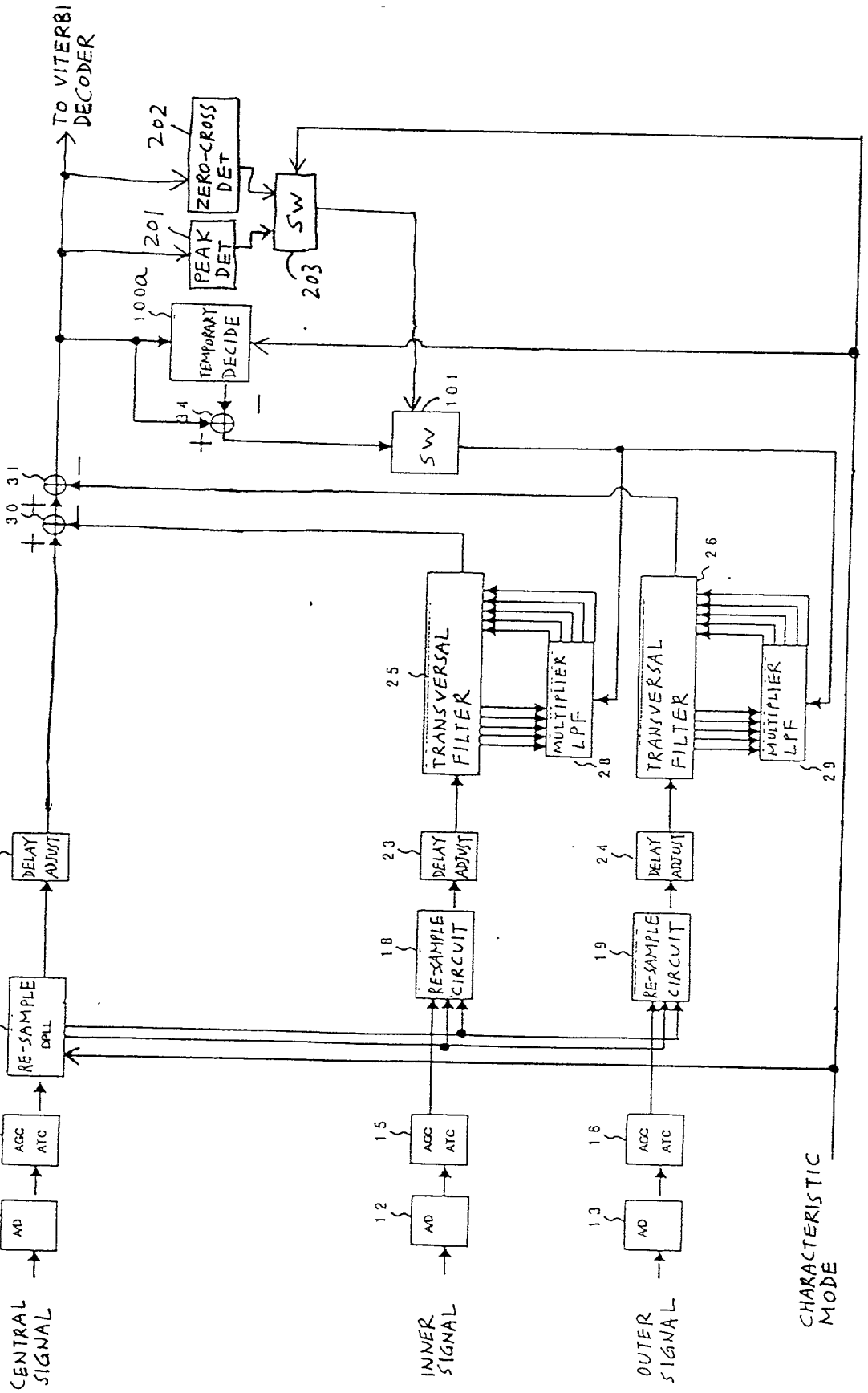

TO VITERBI DECODER
202
ZERO-CROSS DET
201
PEAK DET
SW
203
100a
TEMPORARY DECIDE
34
SW
101
30
31
20
DELAY ADJUST
17a
RE-SAMPLE DPLL
14
AGC ATC
11
A/D
CENTRAL SIGNAL
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
29
23
DELAY ADJUST
18
RE-SAMPLE CIRCUIT
15
AGC ATC
12
A/D
INNER SIGNAL
24
DELAY ADJUST
19
RE-SAMPLE CIRCUIT
16
AGC ATC
13
A/D
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 60

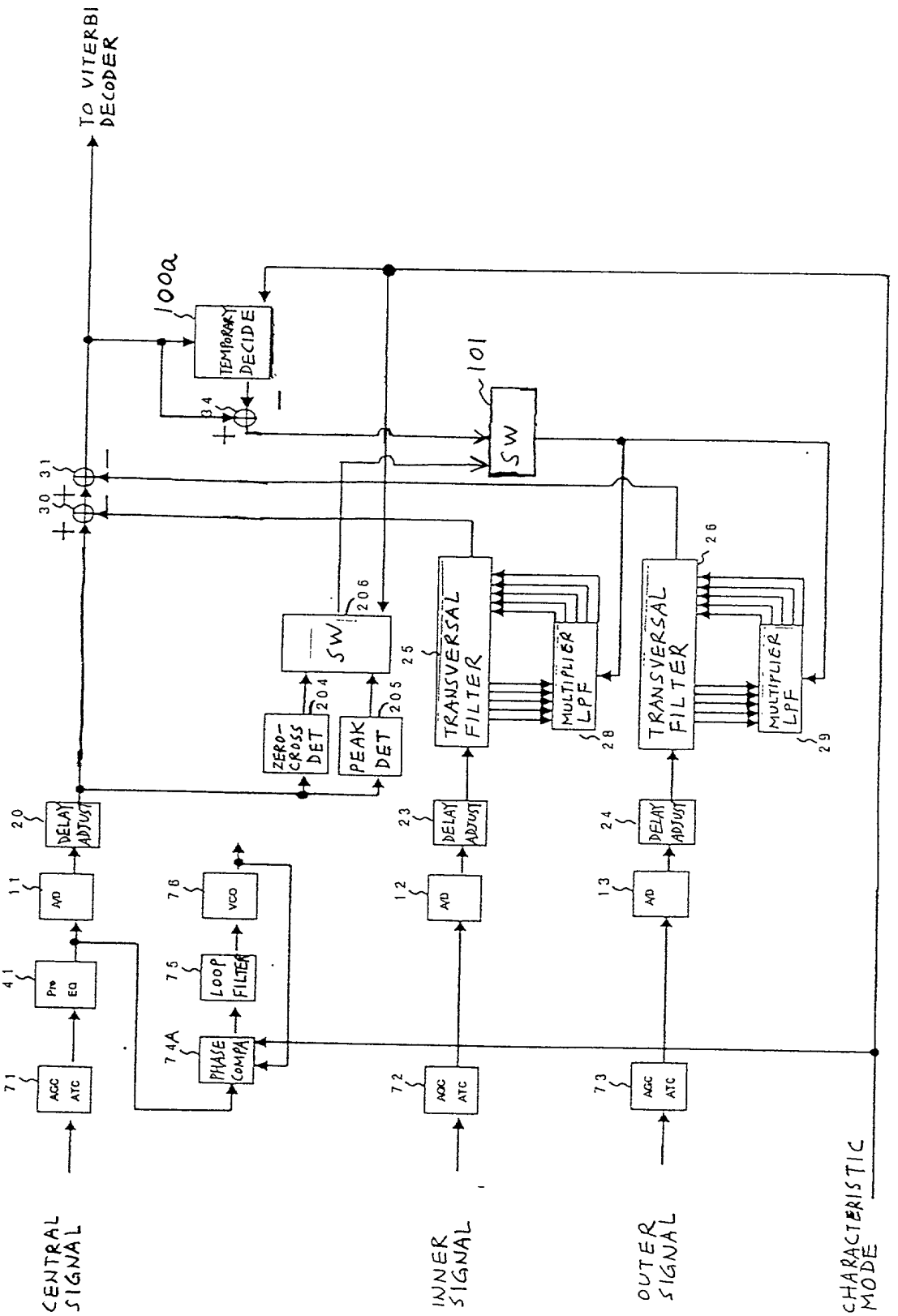

TO VITERBI DECODER
100a
TEMPORARY DECIDE
101
SW
34
30
31
206
ZERO-CROSS DET
204
PEAK DET
205
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
29
20
DELAY ADJUST
11
A/D
41
Pre EQ
71
AGC ATC
76
VCO
75
LOOP FILTER
74A
PHASE COMPA
23
12
72
24
13
73
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 61

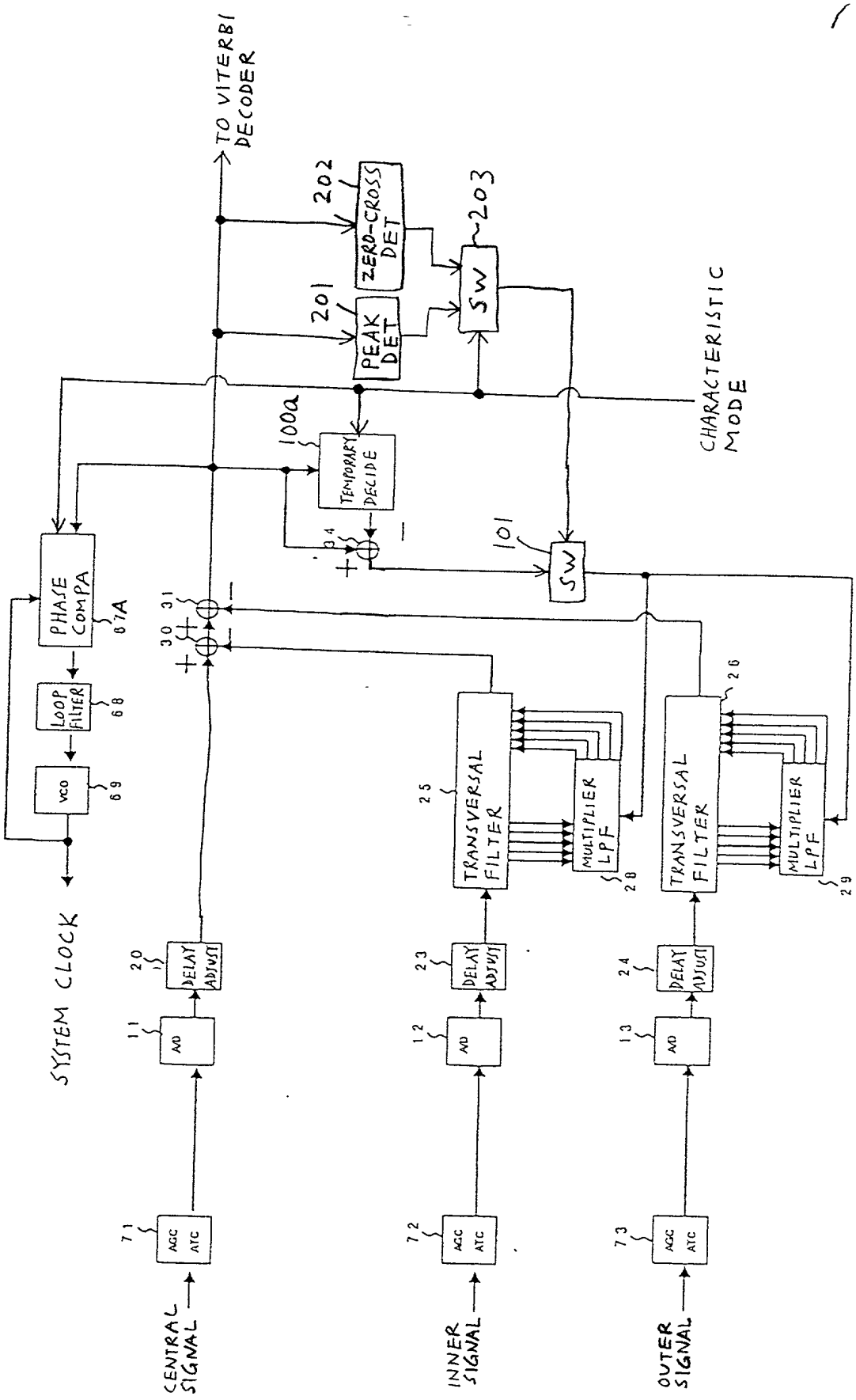

TO VITERBI DECODER
ZERO-CROSS DET
PEAK DET
SW
SW
CHARACTERISTIC MODE
TEMPORARY DECIDE
PHASE COMPA
LOOP FILTER
VCO
SYSTEM CLOCK
DELAY ADJUST
DELAY ADJUST
DELAY ADJUST
A/D
A/D
A/D
AGC ATC
AGC ATC
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
TRANSVERSAL FILTER
TRANSVERSAL FILTER
MULTIPLIER LPF
MULTIPLIER LPF
201
202
203
100a
101
67A
68
69
71
72
73
11
12
13
20
23
24
25
26
28
29
30
31
34

FIG. 62

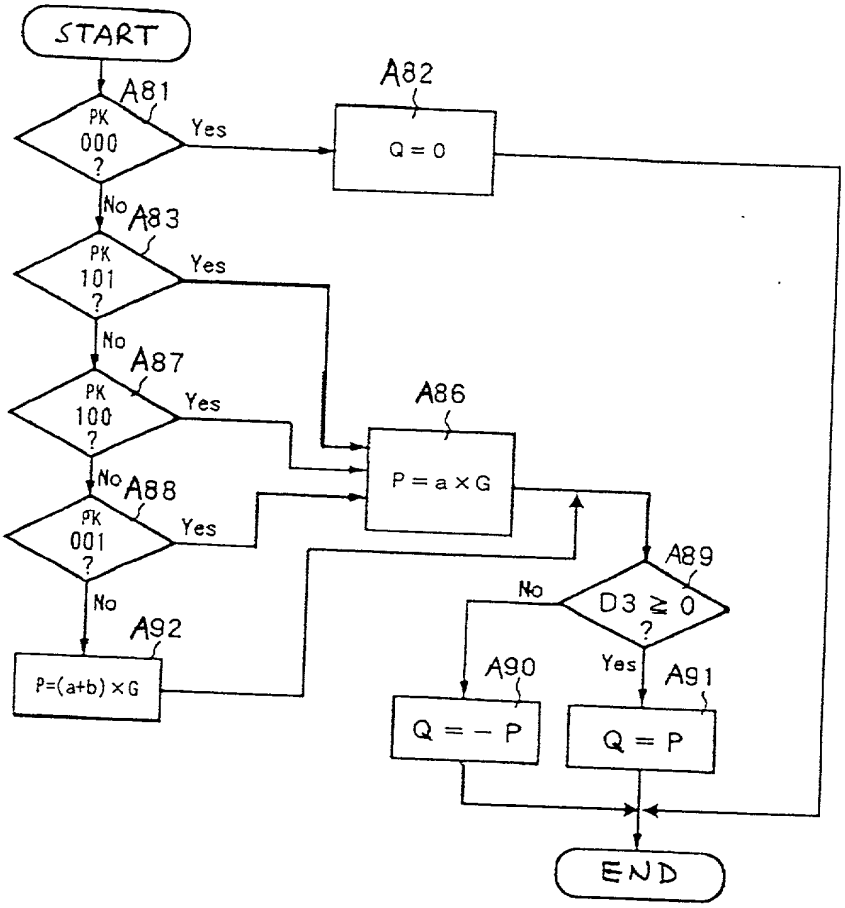
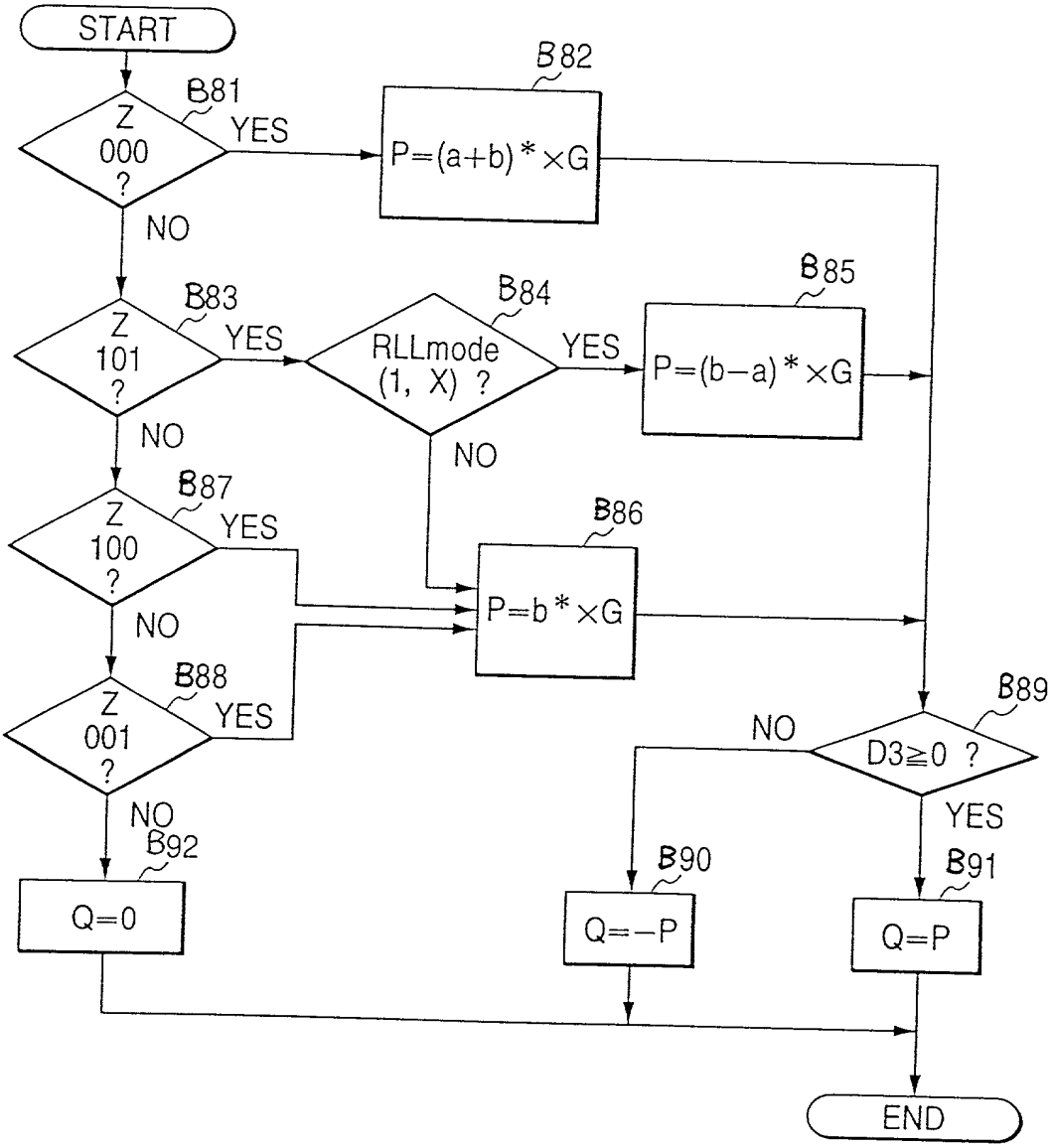

START
A81
PK 000 ?
Yes
A82
Q = 0
No
A83
PK 101 ?
Yes
No
A87
PK 100 ?
Yes
No
A88
PK 001 ?
Yes
No
A92
P=(a+b) × G
A86
P = a × G
A89
D3 ≧ 0 ?
No
Yes
A90
Q = − P
A91
Q = P
END

FIG. 63


START
B81
Z 000 ?
YES
B82
P=(a+b)*×G
NO
B83
Z 101 ?
YES
B84
RLLmode (1, X) ?
YES
B85
P=(b−a)*×G
NO
NO
B87
Z 100 ?
YES
B86
P=b*×G
NO
B88
Z 001 ?
YES
B89
D3≧0 ?
NO
YES
NO
B92
Q=0
B90
Q=−P
B91
Q=P
END